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ATX

Ver: 10

Intel -Kabylake plamform Z270

CPU:

kabylake-S

System Chipset:

Z270

Onboard Chip:

HD Audio Codec:ALC1220
LAN:INTEL I219
SIO:Nuvoton 6795
Flash ROM: SPI 128MB

Main Memory:

*DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)*

ACPI:

NIKO/UPI

PWM:

UPI9508

Expansion Slots:

*PCI Express (X16) Slot *1*
*PCI Express (X8) Slot *1*
*PCI Express (X4) Slot * 1*
*PCI Express (X1) Slot * 3*
*M2 * 2*

Other:

SATA3.0 x6 (PCH)
*FRONT USB2.0 *4*
*FRONTUSB3.0 *4*
*REAR USB3.0 *4*
*REAR USB2.0 *2*
REAR USB TYPE A+C

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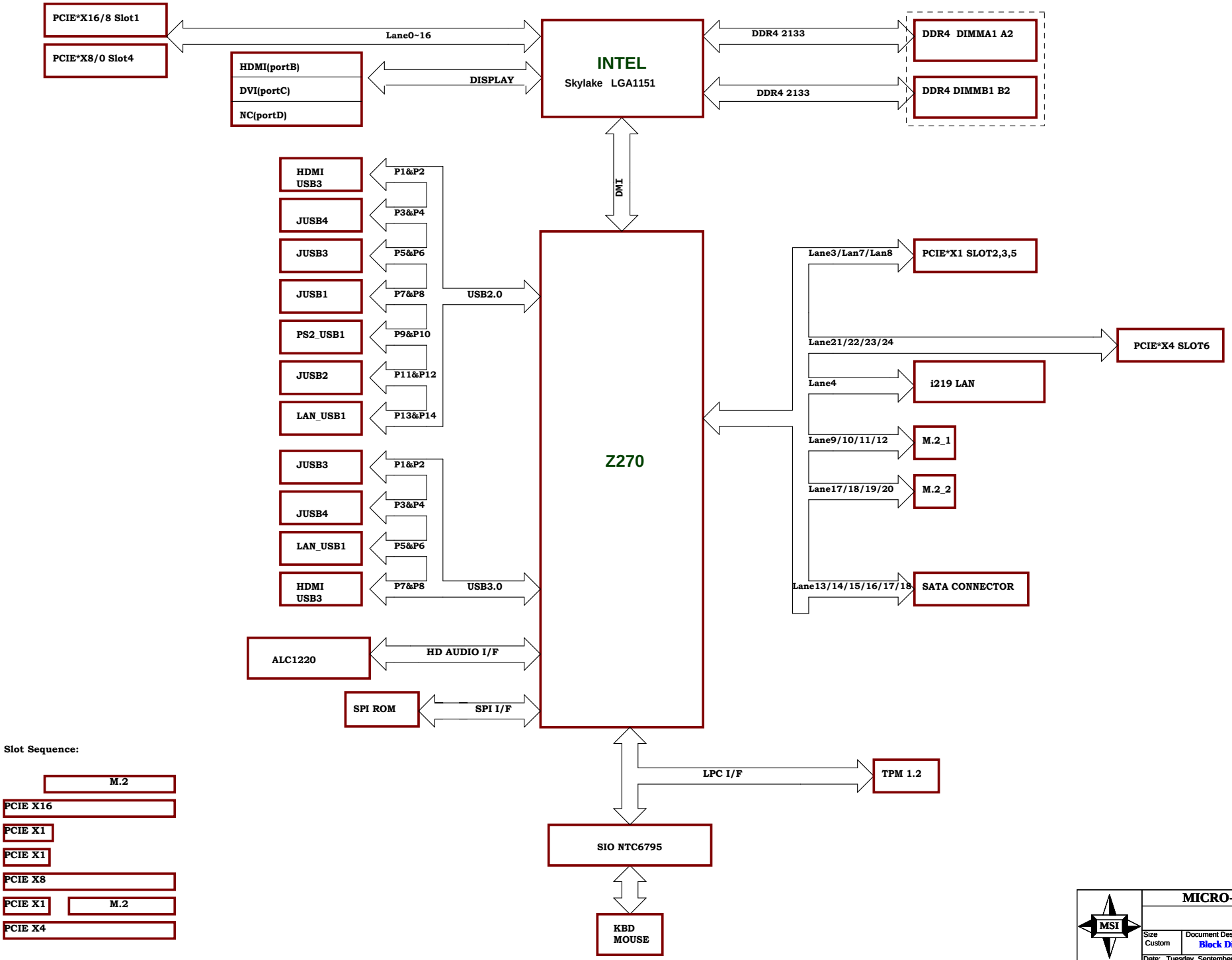
MS-7A63 Block Diagram



Slot Sequence:

- M.2
- PCIE X16
- PCIE X1
- PCIE X1
- PCIE X8
- PCIE X1 / M.2
- PCIE X4

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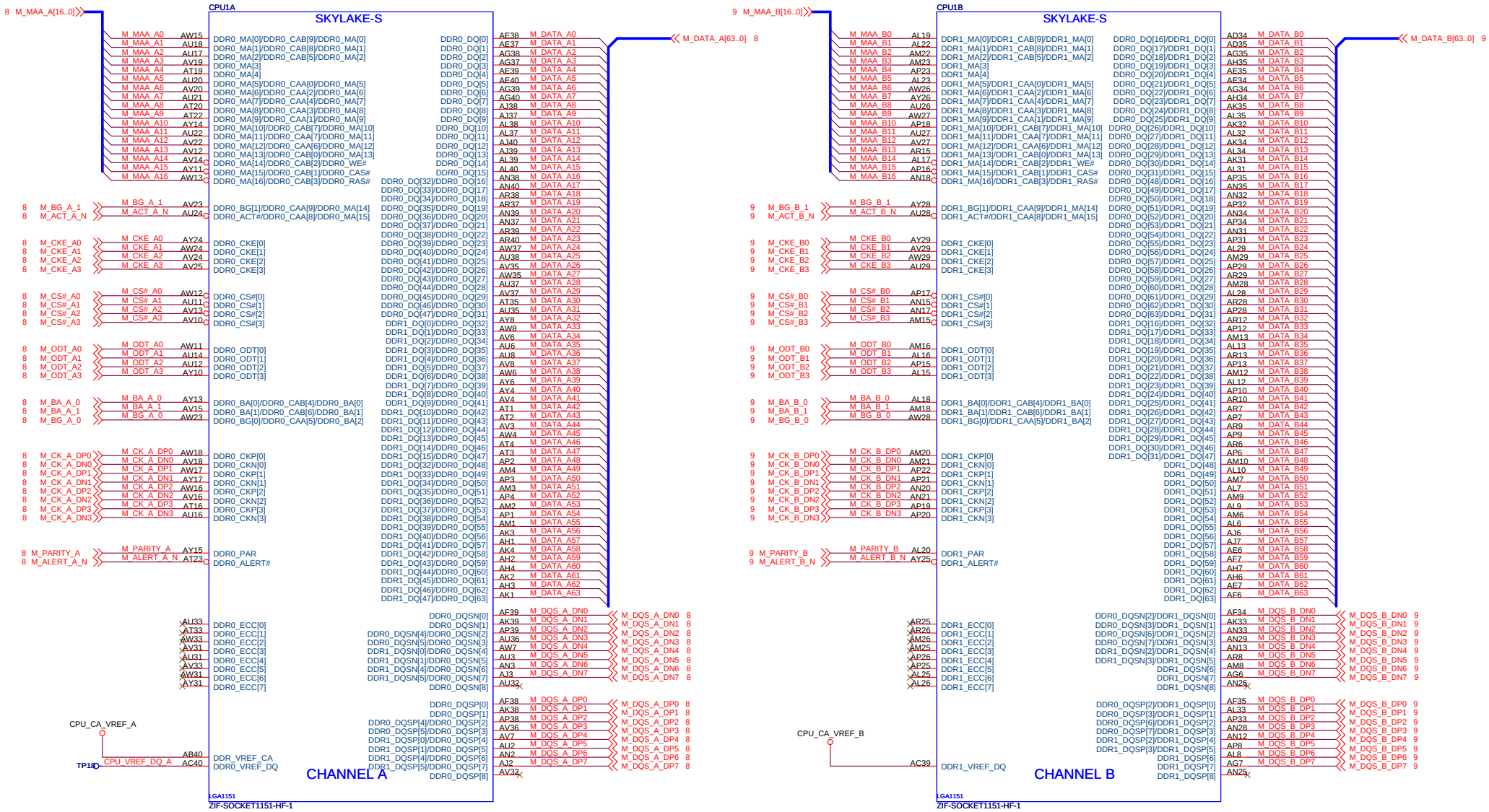

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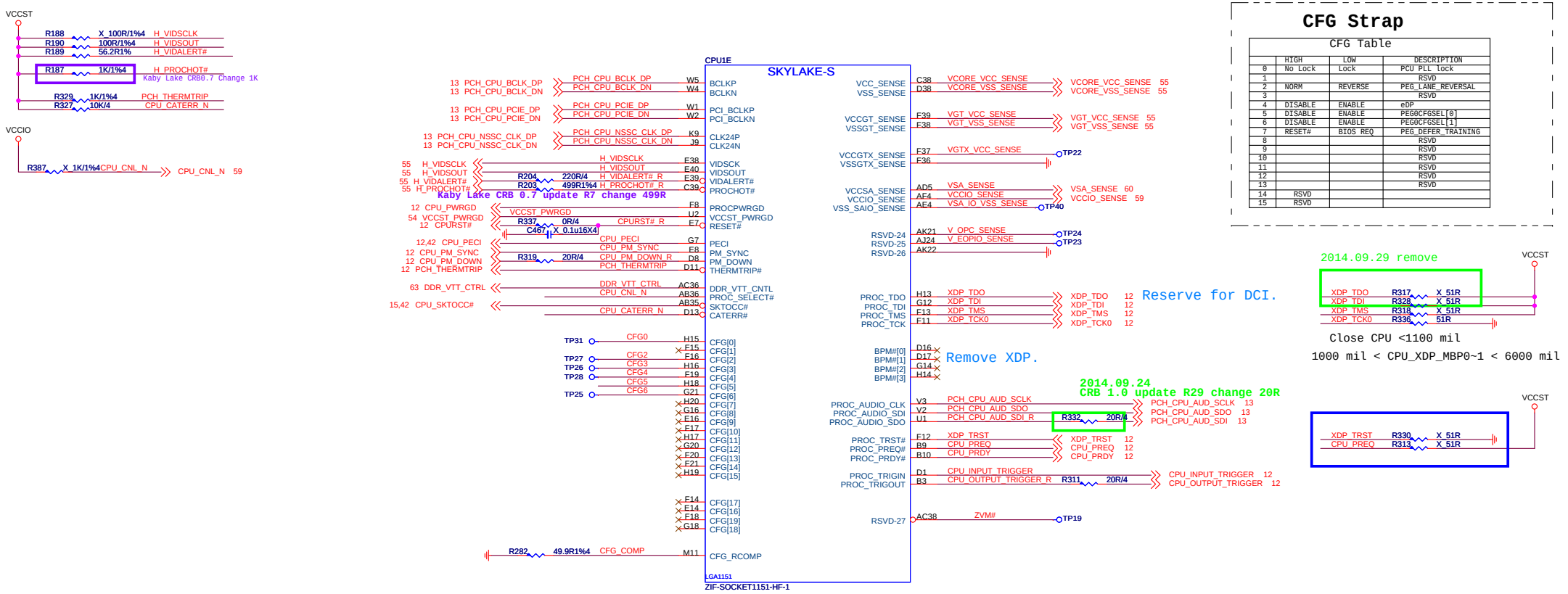
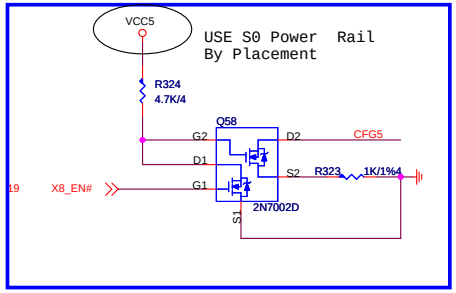
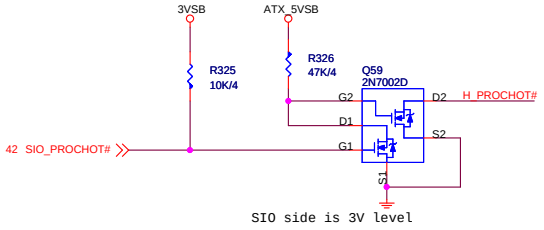


X8 Ctrl

ENABLE# X8	SLOT1	SLOT4
0	X8	X8
1	X16	X0





CFG Strap
CFG Table
HIGH LOW DESCRIPTION
0 No Lock Lock PCU PLL lock
1 RSVD
2 NORM REVERSE PEG_LANE_REVERSAL
3 RSVD
4 DISABLE ENABLE eDP
5 DISABLE ENABLE PEG0CFGSEL[0]
6 DISABLE ENABLE PEG0CFGSEL[1]
7 RESET# BIOS REQ PEG_DEFER_TRAINING
8 RSVD
9 PRESENT NO_PRESENT SVID PRESENT
10 RSVD
11 RSVD
12 RSVD
13 RSVD
14 RSVD
15 RSVD

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Size: Custom | Document Description: CPU-Control/MISC/CFG/Audio | Rev: 10

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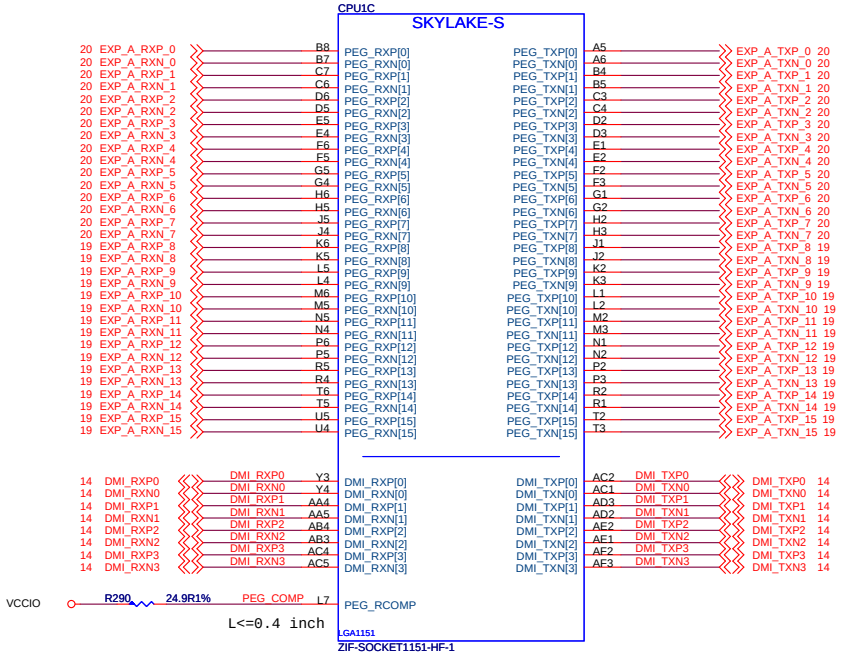

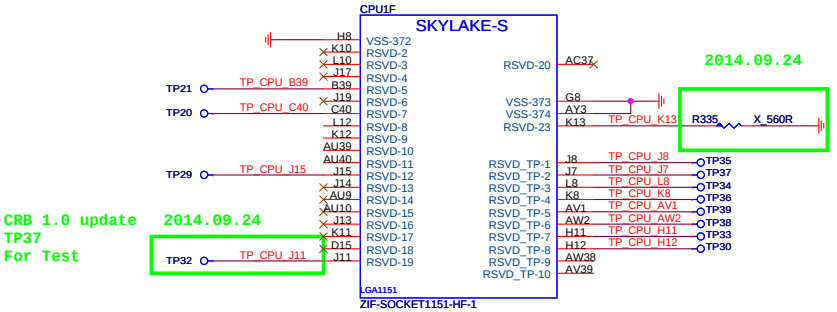

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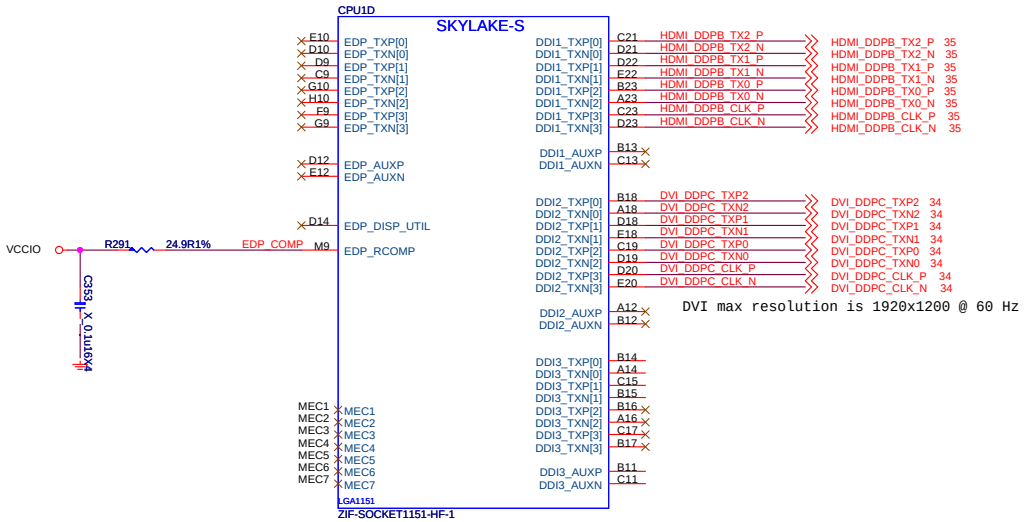

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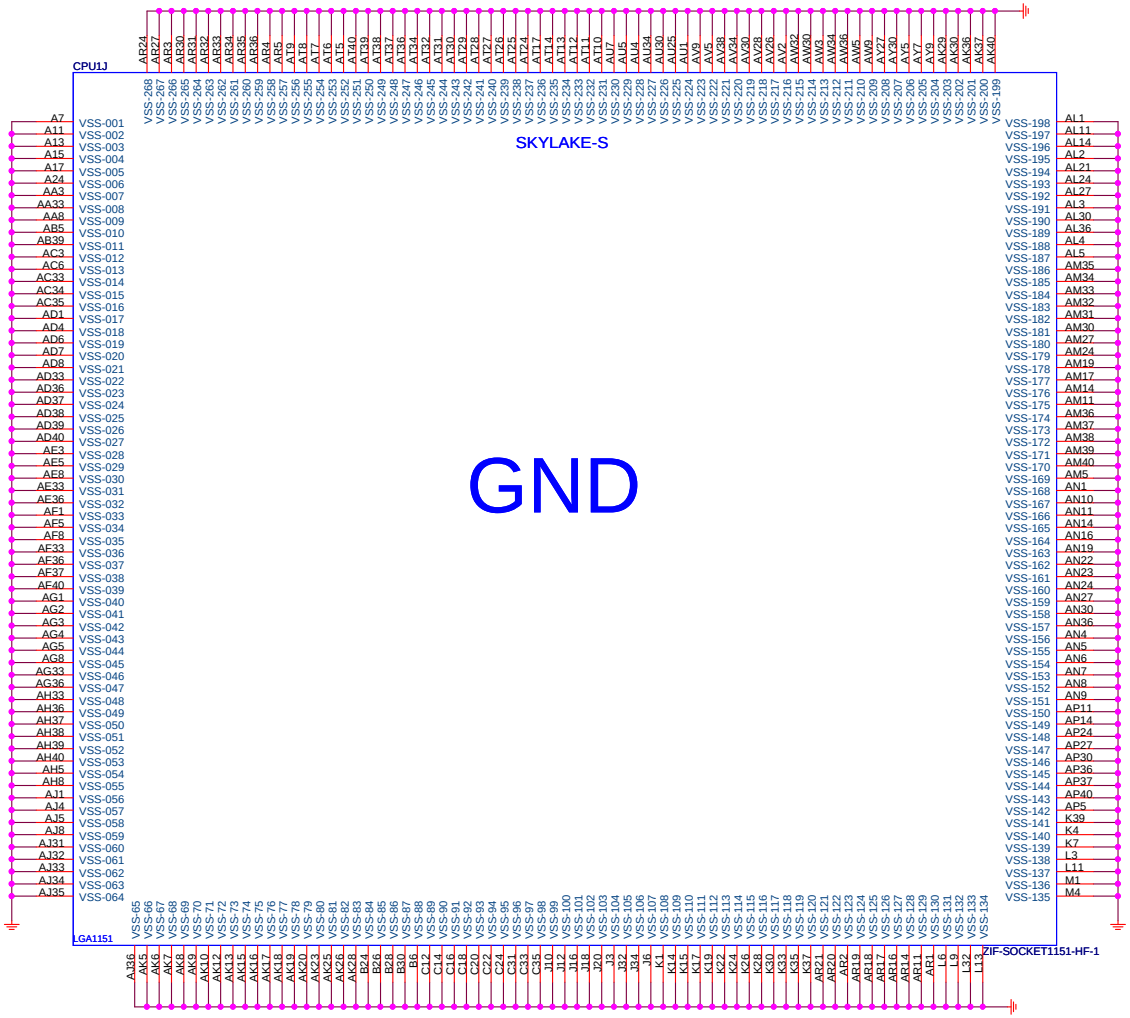

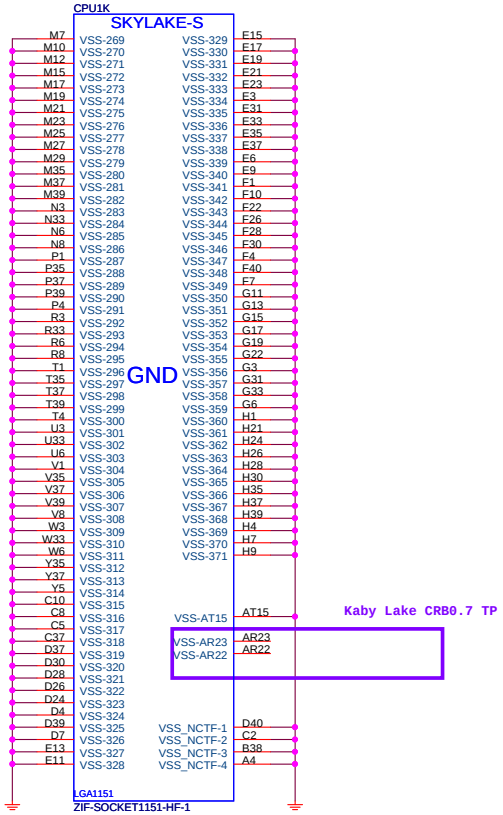

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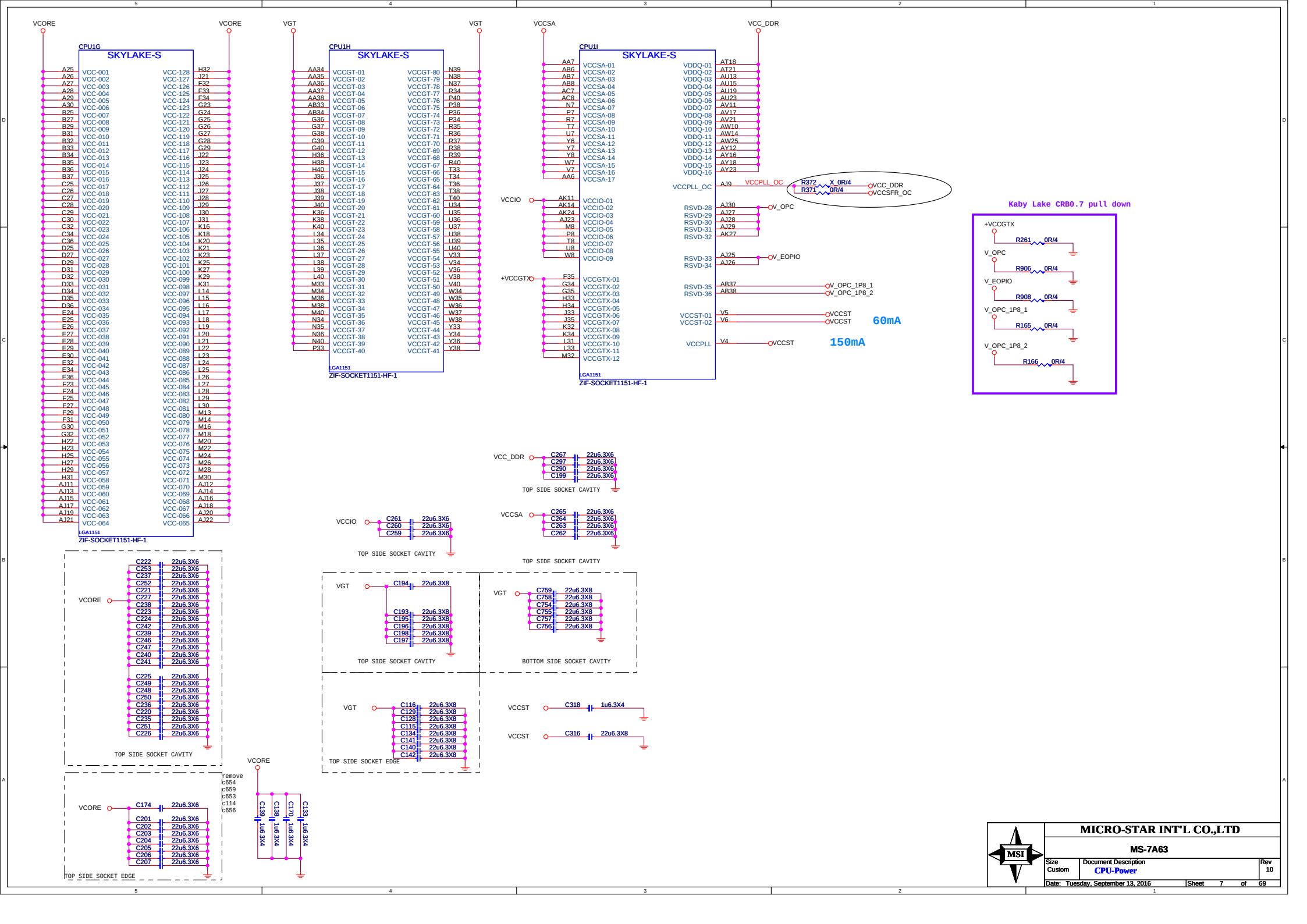
VCORE
CPU1G
SKYLAKE-S
VCC-001 A25
VCC-002 A26
VCC-003 A27
VCC-004 A28
VCC-005 A29
VCC-006 A30
VCC-007 B25
VCC-008 B27
VCC-009 B29
VCC-010 B31
VCC-011 B32
VCC-012 B33
VCC-013 B34
VCC-014 B35
VCC-015 B36
VCC-016 B37
VCC-017 C25
VCC-018 C26
VCC-019 C27
VCC-020 C28
VCC-021 C29
VCC-022 C30
VCC-023 C32
VCC-024 C34
VCC-025 C36
VCC-026 D25
VCC-027 D27
VCC-028 D29
VCC-029 D31
VCC-030 D32
VCC-031 D33
VCC-032 D34
VCC-033 D35
VCC-034 D36
VCC-035 E24
VCC-036 E25
VCC-037 E26
VCC-038 E27
VCC-039 E28
VCC-040 E29
VCC-041 E30
VCC-042 E32
VCC-043 E34
VCC-044 E36
VCC-045 F23
VCC-046 F24
VCC-047 F25
VCC-048 F27
VCC-049 F29
VCC-050 F31
VCC-051 G30
VCC-052 G32
VCC-053 H22
VCC-054 H23
VCC-055 H25
VCC-056 H27
VCC-057 H29
VCC-058 H31
VCC-059 AJ11
VCC-060 AJ13
VCC-061 AJ15
VCC-062 AJ17
VCC-063 AJ19
VCC-064 AJ21
VCC-128 H32
VCC-127 J21
VCC-126 F32
VCC-125 F33
VCC-124 F34
VCC-123 G23
VCC-122 G24
VCC-121 G25
VCC-120 G26
VCC-119 G27
VCC-118 G28
VCC-117 G29
VCC-116 J22
VCC-115 J23
VCC-114 J24
VCC-113 J25
VCC-112 J26
VCC-111 J27
VCC-110 J28
VCC-109 J29
VCC-108 J30
VCC-107 J31
VCC-106 K16
VCC-105 K18
VCC-104 K20
VCC-103 K21
VCC-102 K23
VCC-101 K25
VCC-100 K27
VCC-099 K29
VCC-098 K31
VCC-097 L14
VCC-096 L15
VCC-095 L16
VCC-094 L17
VCC-093 L18
VCC-092 L19
VCC-091 L20
VCC-090 L22
VCC-089 L23
VCC-088 L24
VCC-087 L25
VCC-086 L26
VCC-085 L27
VCC-084 L28
VCC-083 L29
VCC-082 L30
VCC-081 M13
VCC-080 M14
VCC-079 M16
VCC-078 M18
VCC-077 M20
VCC-076 M22
VCC-075 M24
VCC-074 M26
VCC-073 M28
VCC-072 M30
VCC-071 AJ12
VCC-070 AJ14
VCC-069 AJ16
VCC-068 AJ18
VCC-067 AJ20
VCC-066 AJ22
VCC-065
LGA1151
ZIF-SOCKET1151-HF-1
VGT
CPU1H
SKYLAKE-S
VCCGT-01 AA34
VCCGT-02 AA35
VCCGT-03 AA36
VCCGT-04 AA37
VCCGT-05 AA38
VCCGT-06 AB33
VCCGT-07 AB34
VCCGT-08 G36
VCCGT-09 G37
VCCGT-10 G38
VCCGT-11 G39
VCCGT-12 G40
VCCGT-13 H36
VCCGT-14 H38
VCCGT-15 H40
VCCGT-16 J36
VCCGT-17 J37
VCCGT-18 J38
VCCGT-19 J39
VCCGT-20 J40
VCCGT-21 K36
VCCGT-22 K38
VCCGT-23 K40
VCCGT-24 L34
VCCGT-25 L35
VCCGT-26 L36
VCCGT-27 L37
VCCGT-28 L38
VCCGT-29 L39
VCCGT-30 L40
VCCGT-31 M33
VCCGT-32 M34
VCCGT-33 M36
VCCGT-34 M38
VCCGT-35 M40
VCCGT-36 N34
VCCGT-37 N35
VCCGT-38 N36
VCCGT-39 N40
VCCGT-40 P33
VCCGT-80 N39
VCCGT-79 N38
VCCGT-78 N37
VCCGT-77 R34
VCCGT-76 P40
VCCGT-75 P38
VCCGT-74 P36
VCCGT-73 P34
VCCGT-72 R35
VCCGT-71 R36
VCCGT-70 R37
VCCGT-69 R38
VCCGT-68 R39
VCCGT-67 R40
VCCGT-66 T33
VCCGT-65 T34
VCCGT-64 T36
VCCGT-63 T38
VCCGT-62 T40
VCCGT-61 U34
VCCGT-60 U35
VCCGT-59 U36
VCCGT-58 U37
VCCGT-57 U38
VCCGT-56 U39
VCCGT-55 U40
VCCGT-54 V33
VCCGT-53 V34
VCCGT-52 V36
VCCGT-51 V38
VCCGT-50 V40
VCCGT-49 W34
VCCGT-48 W35
VCCGT-47 W36
VCCGT-46 W37
VCCGT-45 W38
VCCGT-44 Y33
VCCGT-43 Y34
VCCGT-42 Y36
VCCGT-41 Y38
LGA1151
ZIF-SOCKET1151-HF-1
VCCSA
VCC_DDR
CPU1I
SKYLAKE-S
VCCSA-01 AA7
VCCSA-02 AB6
VCCSA-03 AB7
VCCSA-04 AB8
VCCSA-05 AC7
VCCSA-06 AC8
VCCSA-07 N7
VCCSA-08 P7
VCCSA-09 R7
VCCSA-10 T7
VCCSA-11 U7
VCCSA-12 Y6
VCCSA-13 Y7
VCCSA-14 Y8
VCCSA-15 W7
VCCSA-16 V7
VCCSA-17 AA6
VCCIO-01 AK11
VCCIO-02 AK14
VCCIO-03 AK24
VCCIO-04 AJ23
VCCIO-05 M8
VCCIO-06 P8
VCCIO-07 T8
VCCIO-08 U8
VCCIO-09 W8
VCCGTX-01 F35
VCCGTX-02 G34
VCCGTX-03 G35
VCCGTX-04 H33
VCCGTX-05 H34
VCCGTX-06 J33
VCCGTX-07 J35
VCCGTX-08 K32
VCCGTX-09 K34
VCCGTX-10 L31
VCCGTX-11 L33
VCCGTX-12 M32
VDDQ-01 AT18
VDDQ-02 AT21
VDDQ-03 AU13
VDDQ-04 AU15
VDDQ-05 AU19
VDDQ-06 AU23
VDDQ-07 AV11
VDDQ-08 AV17
VDDQ-09 AV21
VDDQ-10 AW10
VDDQ-11 AW14
VDDQ-12 AW25
VDDQ-13 AY12
VDDQ-14 AY16
VDDQ-15 AY18
VDDQ-16 AY23
VCCPLL_OC AJ9
RSVD-28 AJ30
RSVD-29 AJ27
RSVD-30 AJ28
RSVD-31 AJ29
RSVD-32 AK27
RSVD-33 AJ25
RSVD-34 AJ26
RSVD-35 AB37
RSVD-36 AB38
VCCST-01 V5
VCCST-02 V6
VCCPLL V4
LGA1151
ZIF-SOCKET1151-HF-1
VCCPLL_OC
R372 X_0R/4
R371 0R/4
VCC_DDR
VCCSFR_OC
V_OPC
V_EOPIO
V_OPC_1P8_1
V_OPC_1P8_2
VCCST
VCCST
60mA
VCCST
150mA
Kaby Lake CRB0.7 pull down
+VCCGTX
R261 0R/4
V_OPC
R906 0R/4
V_EOPIO
R908 0R/4
V_OPC_1P8_1
R165 0R/4
V_OPC_1P8_2
R166 0R/4
VCC_DDR
C267 22u6.3X6
C297 22u6.3X6
C290 22u6.3X6
C199 22u6.3X6
TOP SIDE SOCKET CAVITY
VCCIO
C261 22u6.3X6
C260 22u6.3X6
C259 22u6.3X6
TOP SIDE SOCKET CAVITY
VCCSA
C265 22u6.3X6
C264 22u6.3X6
C263 22u6.3X6
C262 22u6.3X6
TOP SIDE SOCKET CAVITY
VCORE
C222 22u6.3X6
C253 22u6.3X6
C237 22u6.3X6
C252 22u6.3X6
C221 22u6.3X6
C227 22u6.3X6
C238 22u6.3X6
C223 22u6.3X6
C224 22u6.3X6
C242 22u6.3X6
C239 22u6.3X6
C246 22u6.3X6
C247 22u6.3X6
C240 22u6.3X6
C241 22u6.3X6
C225 22u6.3X6
C249 22u6.3X6
C248 22u6.3X6
C250 22u6.3X6
C236 22u6.3X6
C220 22u6.3X6
C235 22u6.3X6
C251 22u6.3X6
C226 22u6.3X6
TOP SIDE SOCKET CAVITY
VGT
C194 22u6.3X8
C193 22u6.3X8
C195 22u6.3X8
C196 22u6.3X8
C198 22u6.3X8
C197 22u6.3X8
TOP SIDE SOCKET CAVITY
VGT
C759 22u6.3X8
C758 22u6.3X8
C754 22u6.3X8
C755 22u6.3X8
C757 22u6.3X8
C756 22u6.3X8
BOTTOM SIDE SOCKET CAVITY
VGT
C116 22u6.3X8
C129 22u6.3X8
C128 22u6.3X8
C115 22u6.3X8
C134 22u6.3X8
C141 22u6.3X8
C140 22u6.3X8
C142 22u6.3X8
TOP SIDE SOCKET EDGE
VCCST
C318 1u6.3X4
VCCST
C316 22u6.3X8
VCORE
C174 22u6.3X6
C201 22u6.3X6
C202 22u6.3X6
C203 22u6.3X6
C204 22u6.3X6
C205 22u6.3X6
C206 22u6.3X6
C207 22u6.3X6
TOP SIDE SOCKET EDGE
remove
c654
c659
c653
c114
c656
VCORE
C139 1u6.3X4
C138 1u6.3X4
C170 1u6.3X4
C133 1u6.3X4
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MS-7A63
Size
Custom
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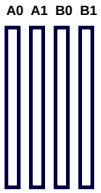

VCC_DDR

DIMMA1A

M_DATA_A[63..0] 3

M_DQS_A_DP7 3
M_DQS_A_DN7 3
M_DQS_A_DP6 3
M_DQS_A_DN6 3
M_DQS_A_DP5 3
M_DQS_A_DN5 3
M_DQS_A_DP4 3
M_DQS_A_DN4 3
M_DQS_A_DP3 3
M_DQS_A_DN3 3
M_DQS_A_DP2 3
M_DQS_A_DN2 3
M_DQS_A_DP1 3
M_DQS_A_DN1 3
M_DQS_A_DP0 3
M_DQS_A_DN0 3

M_CK_A_DP1 3
M_CK_A_DN1 3
M_CK_A_DP0 3
M_CK_A_DN0 3

M_CS#_A1 3
M_CS#_A0 3
M_CKE_A1 3
M_CKE_A0 3
M_ODT_A1 3
M_ODT_A0 3

M_BG_A_1 3
M_BG_A_0 3
M_BA_A_1 3
M_BA_A_0 3

M_MAA_A[16..0]
M_MAA_A[16..0] 3

M_ALERT_A_N 3
M_ACT_A_N 3
M_PARITY_A 3

DIMM_RESET#
DIMM1_EVENT

SMB_CLK_DIMM
SMB_DATA_DIMM

DDRIV-288P_BLACK-RH-21

DIMM1(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

VCC_DDR

DIMMA2A

M_CK_A_DP3 3
M_CK_A_DN3 3
M_CK_A_DP2 3
M_CK_A_DN2 3

M_CS#_A3 3
M_CS#_A2 3
M_CKE_A3 3
M_CKE_A2 3
M_ODT_A3 3
M_ODT_A2 3

DIMM2_EVENT

DDRIV-288P_BLACK-RH-21

DIMM2(CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]

VCC_DDR

DIMM1_EVENT R283 240R1%4
DIMM2_EVENT R284 240R1%4

VCC_DDR

R254 470R1%4

12 DRAM_RESET# R252 0R/4 DIMM_RESET# DIMM_RESET# 9

C175 X_0.1u16X4

12,23,38,55 SMBCLK_VCC SMBCLK_VCC R390 0R/4 SMB_CLK_DIMM SMB_CLK_DIMM 9
12,23,38,55 SMBDATA_VCC SMBDATA_VCC R389 0R/4 SMB_DATA_DIMM SMB_DATA_DIMM 9

VDDSPD

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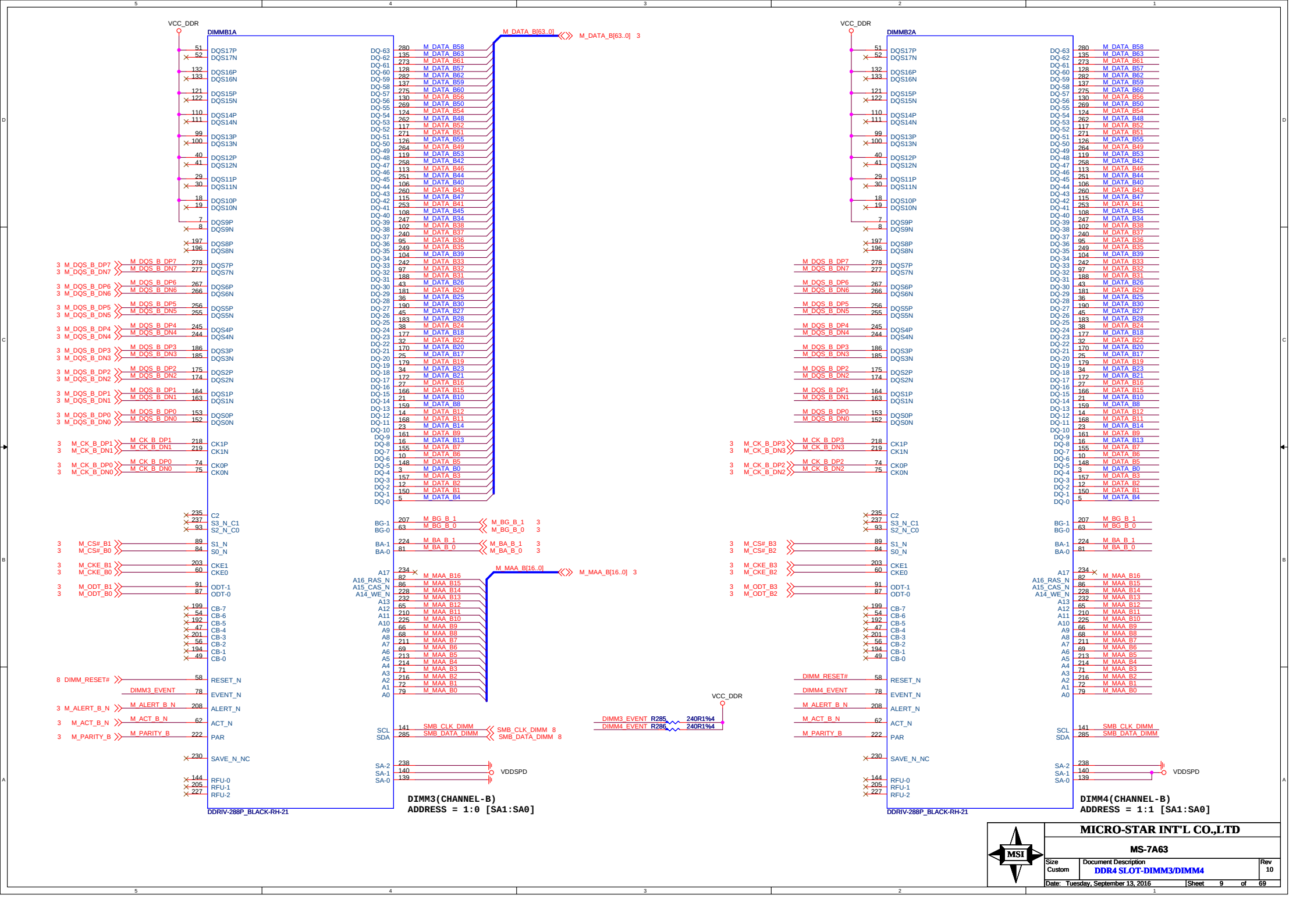

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Size: Custom	Document Description: DDR4 SLOT-DIMM3/DIMM4	Rev: 10
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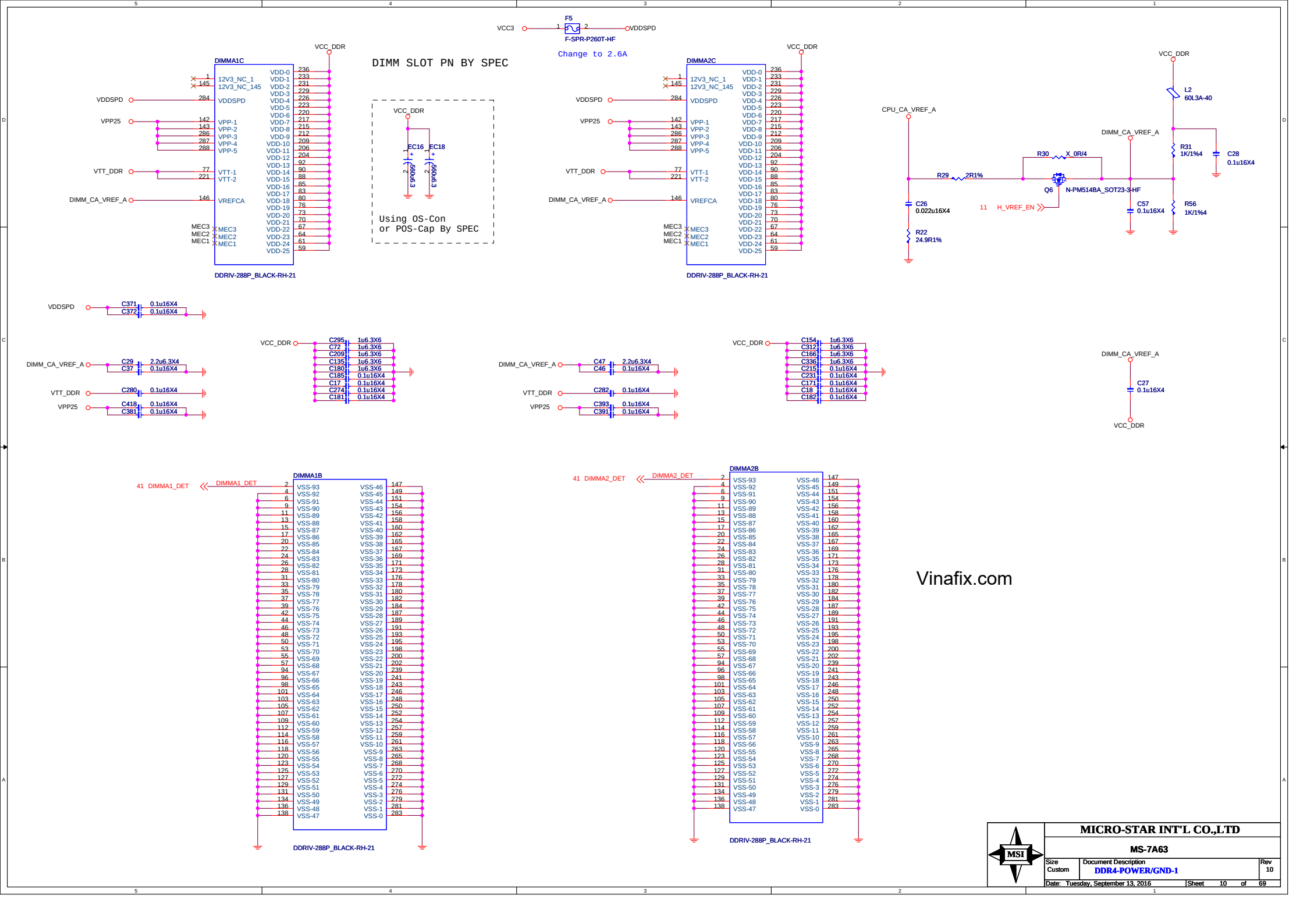
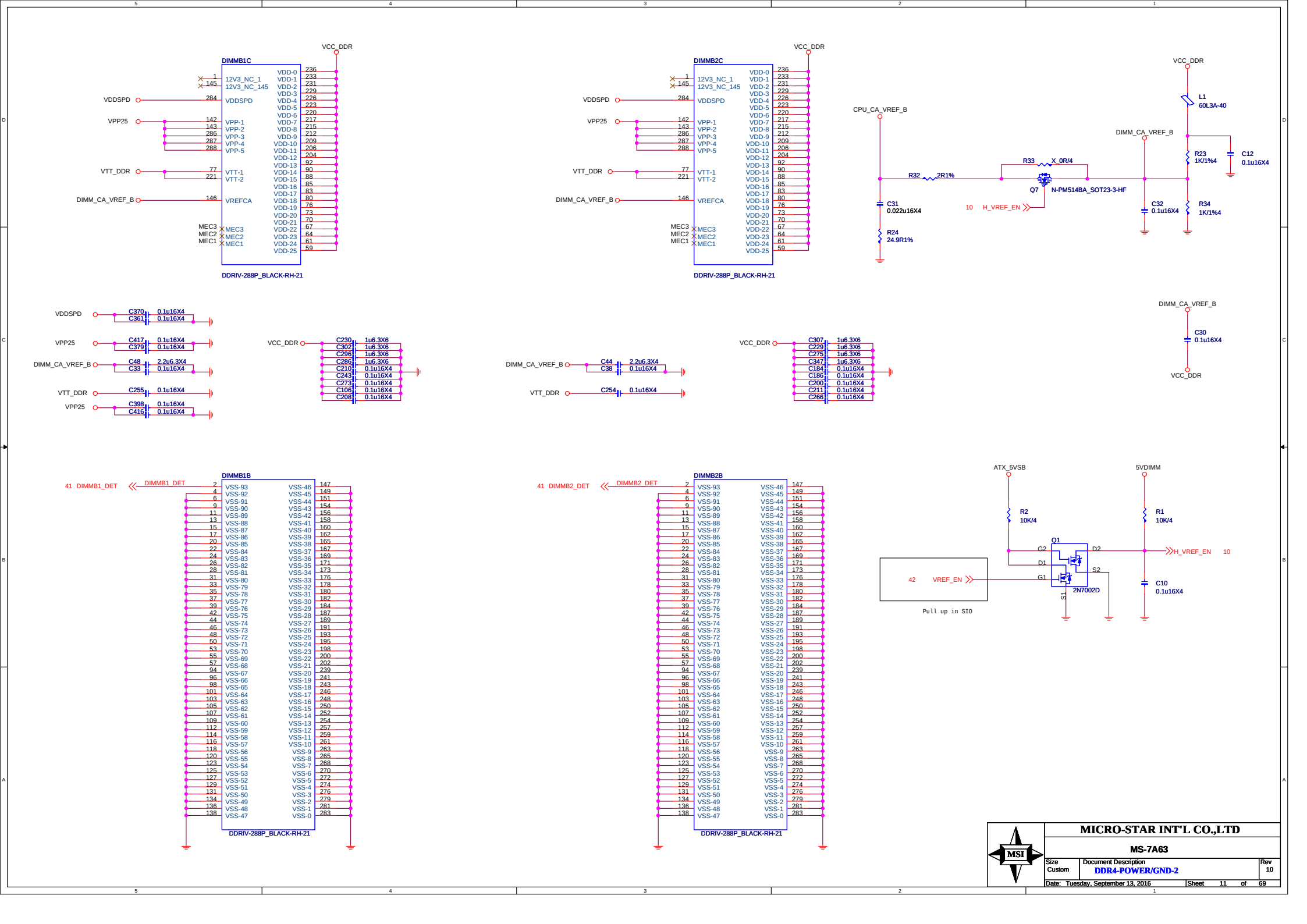

F5
VCC3
VDDSPD
F-SPR-P260T-HF
DIMM SLOT PN BY SPEC
Change to 2.6A
DIMMA1C
DIMMA2C
VCC_DDR
VDDSPD
VPP25
VTT_DDR
DIMM_CA_VREF_A
DDRIV-288P_BLACK-RH-21
EC16
EC18
560u6.3
Using OS-Con
or POS-Cap By SPEC
CPU_CA_VREF_A
L2
60L3A-40
R30
X_0R/4
R29
2R1%
Q6
N-PM514BA_SOT23-3-HF
R31
1K/1%4
C28
0.1u16X4
C26
0.022u16X4
11
H_VREF_EN
C57
0.1u16X4
R56
1K/1%4
R22
24.9R1%
C371
C372
0.1u16X4
C29
C37
2.2u6.3X4
C280
C418
C381
C295
C72
C209
C135
C180
C185
C17
C274
C181
1u6.3X6
C47
C46
C282
C393
C391
C154
C312
C166
C336
C215
C231
C171
C18
C182
C27
DIMMA1B
DIMMA2B
41 DIMMA1_DET
DIMMA1_DET
41 DIMMA2_DET
DIMMA2_DET
Vinafix.com
MICRO-STAR INT'L CO.,LTD
MS-7A63
Size
Custom
Document Description
DDR4-POWER/GND-1
Rev
10
Date: Tuesday, September 13, 2016
Sheet 10 of 69


DIMMB1C
DDRIV-288P_BLACK-RH-21
VCC_DDR
VDDSPD
VPP25
VTT_DDR
DIMM_CA_VREF_B
DIMMB2C
DDRIV-288P_BLACK-RH-21
CPU_CA_VREF_B
L1
60L3A-40
R23
1K/1%4
C12
0.1u16X4
R33
X_0R/4
R32
2R1%
Q7
N-PM514BA_SOT23-3-HF
C31
0.022u16X4
10
H_VREF_EN
C32
0.1u16X4
R34
1K/1%4
R24
24.9R1%
C370
C361
C417
C379
C48
C33
C255
C398
C416
C230
C302
C296
C286
C210
C243
C273
C106
C208
C44
C38
C254
C307
C229
C275
C347
C184
C186
C200
C211
C266
C30
DIMMB1B
41
DIMMB1_DET
DIMMB2B
41
DIMMB2_DET
ATX_5VSB
5VDIMM
R2
10K/4
R1
10K/4
Q1
2N7002D
42
VREF_EN
Pull up in SIO
C10
0.1u16X4
MICRO-STAR INT'L CO.,LTD
MS-7A63
Size
Custom
Document Description
DDR4-POWER/GND-2
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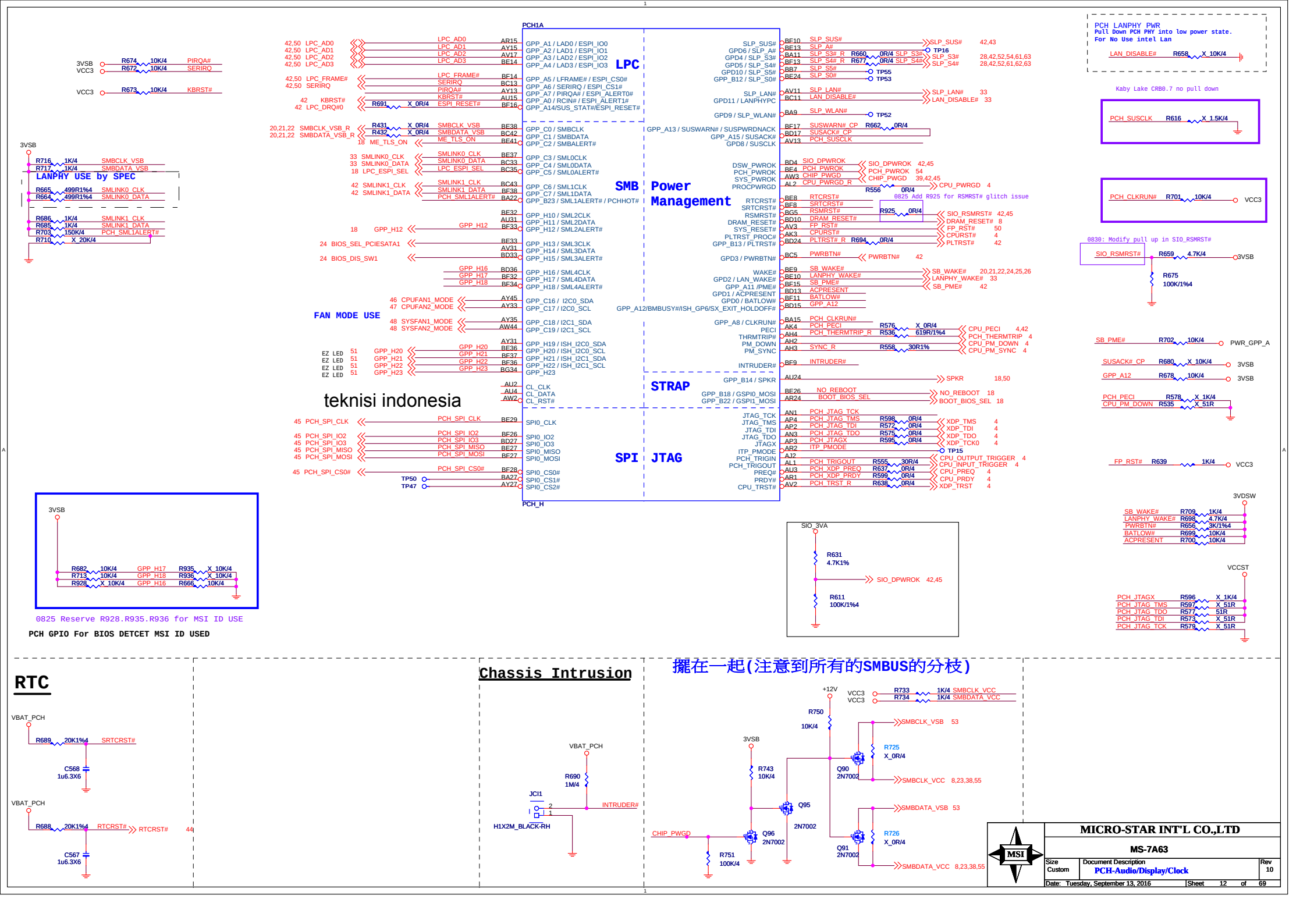
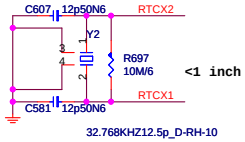
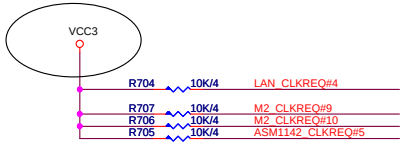

PCH1A
LPC
SMB
Power Management
STRAP
SPI
JTAG
PCH_H
FAN MODE USE
teknisi indonesia
LANPHY USE by SPEC
PCH_LANPHY_PWR
Pull Down PCH PHY into low power state.
For No Use intel Lan
Kaby Lake CRB0.7 no pull down
0825 Reserve R928.R935.R936 for MSI ID USE
PCH GPIO For BIOS DETCET MSI ID USED
RTC
Chassis Intrusion
擺在一起(注意到所有的SMBUS的分枝)
MICRO-STAR INT'L CO.,LTD
MS-7A63
PCH-Audio/Display/Clock

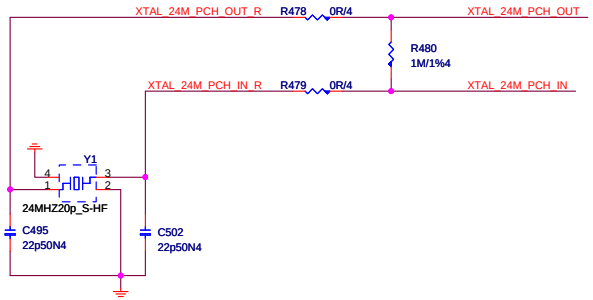
PCH_CLK

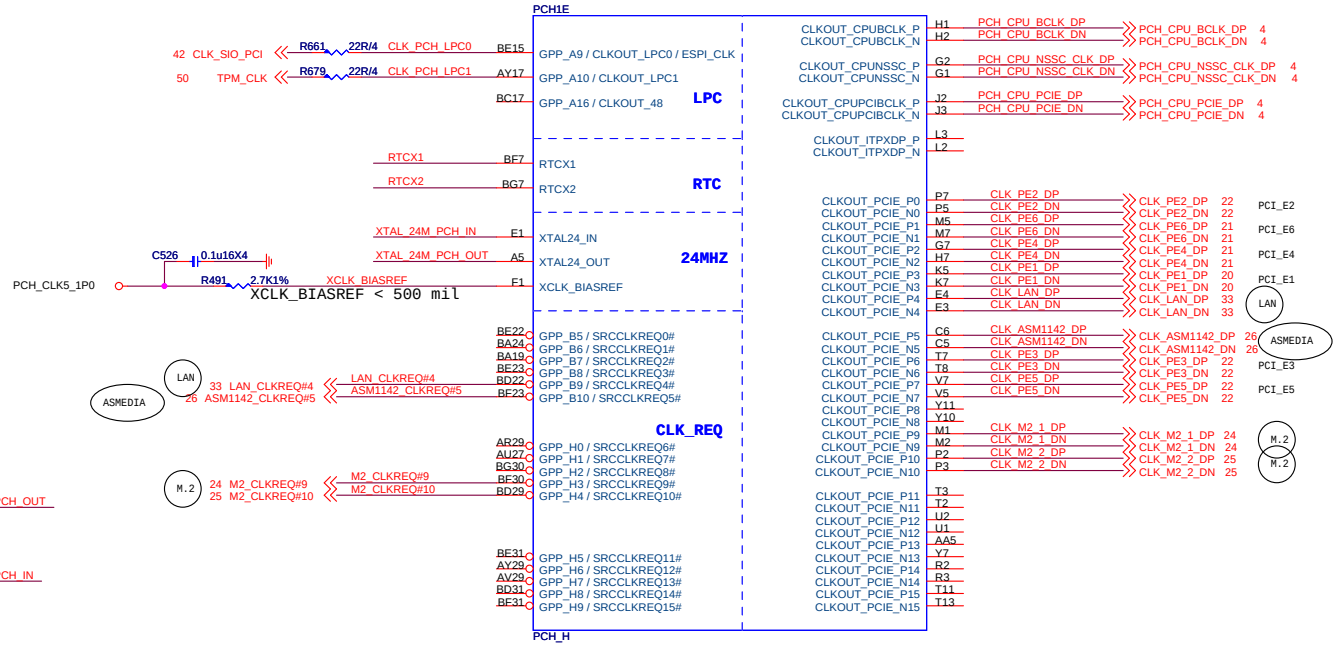
RTC_Block

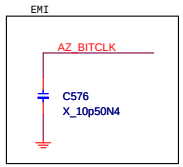
Close to PCH

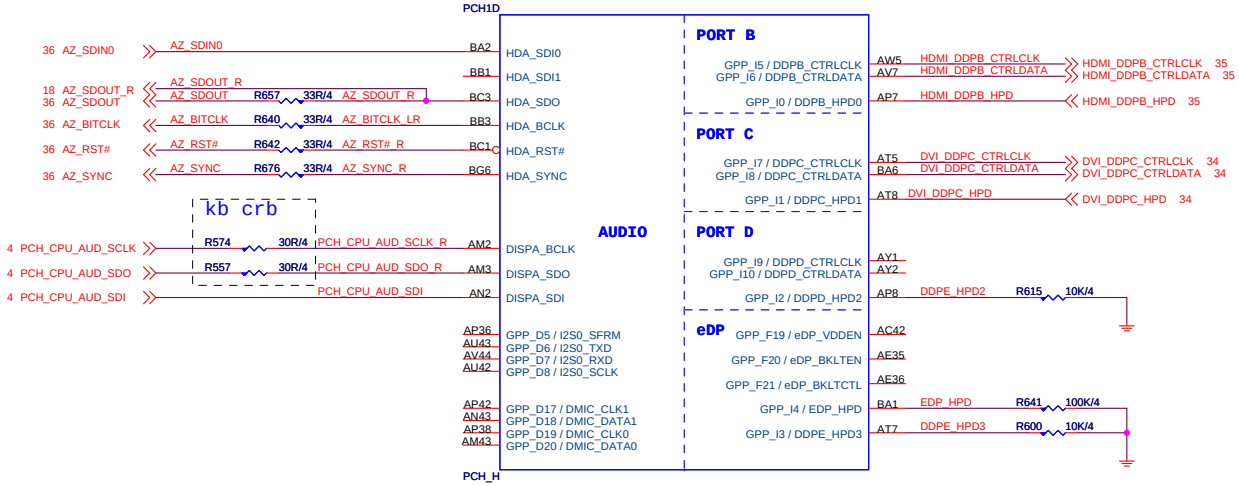


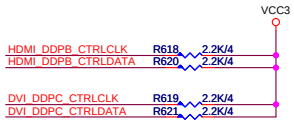












MICRO-STAR INT'L CO.,LTD

MS-7A63

Size	Document Description	Rev
Custom	PCH-USB/PCIE/DMI/SATA	10

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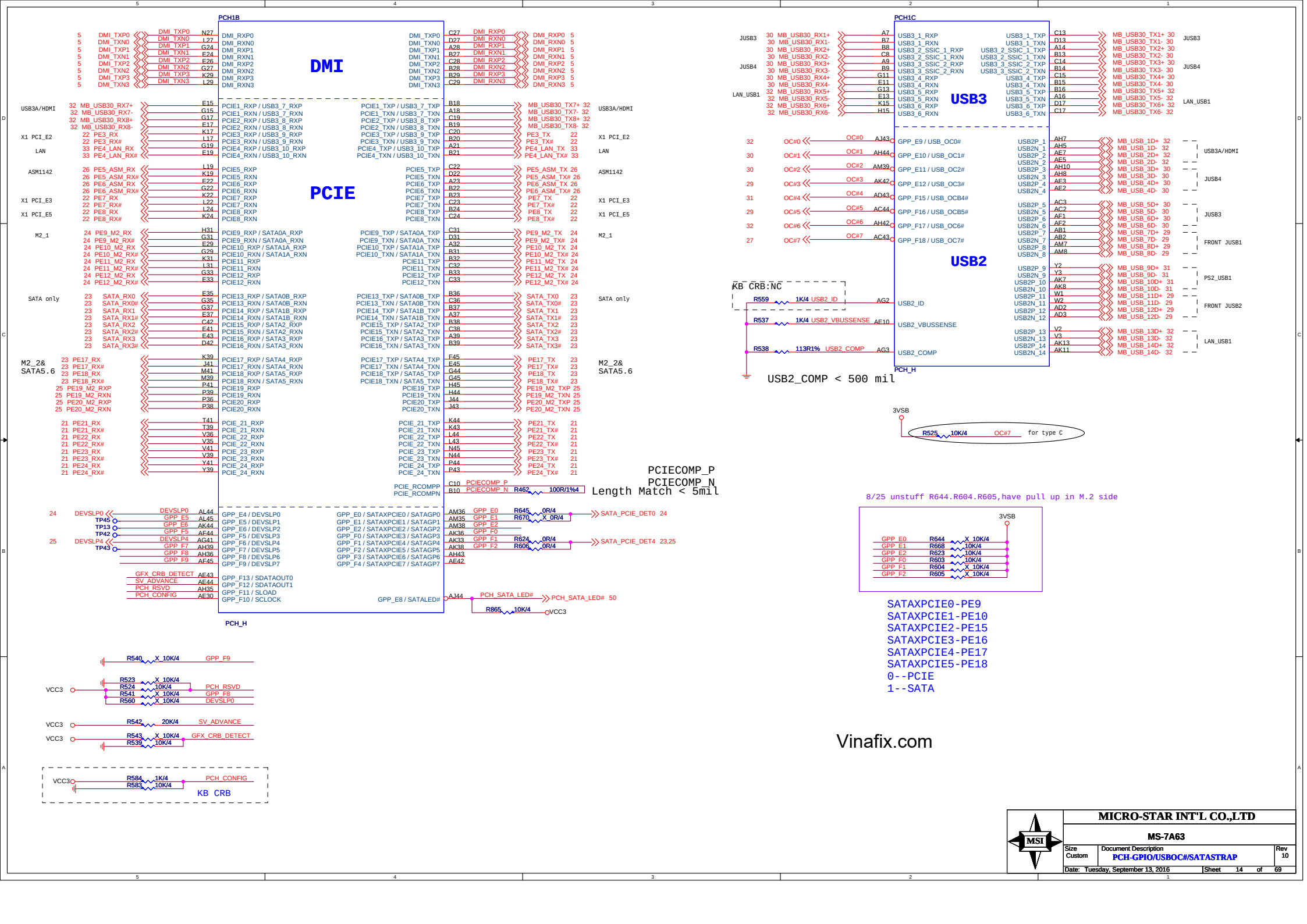
PCH1B
DMI
PCIE
PCH_H
PCH1C
USB3
USB2
KB CRB:NC
R559 1K/4 USB2_ID
R537 1K/4 USB2_VBUSSENSE
R538 113R1% USB2_COMP
USB2_COMP < 500 mil
3VSB
R525 10K/4 OC#7 for type C
PCIECOMP_P
PCIECOMP_N
R462 100R/1%4
Length Match < 5mil
8/25 unstuff R644.R604.R605,have pull up in M.2 side
SATAXPCIE0-PE9
SATAXPCIE1-PE10
SATAXPCIE2-PE15
SATAXPCIE3-PE16
SATAXPCIE4-PE17
SATAXPCIE5-PE18
0--PCIE
1--SATA
R540 X_10K/4 GPP_F9
R523 X_10K/4
R524 10K/4 PCH_RSVD
R541 X_10K/4 GPP_F8
R560 X_10K/4 DEVSLP0
R542 20K/4 SV_ADVANCE
R543 X_10K/4 GFX_CRB_DETECT
R539 10K/4
R584 1K/4 PCH_CONFIG
R583 10K/4
KB CRB
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MICRO-STAR INT'L CO.,LTD
MS-7A63
Size Custom
Document Description PCH-GPIO/USBOC#/SATASTRAP
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GPP_A18	
0	SATA1
1	M2_1

GPP_A20	
0	M2_2
1	SATA5

0825 Add GPP_A18,GPP_A20 for BIOS Detect M.2 SATA
or on board SATA

PCH1F

24 GPP_A18 — GPP_A18 — BE17 GPP_A17 / ISH_GP7
BD19 GPP_A18 / ISH_GP0
23 GPP_A20 — GPP_A20 — BE18 GPP_A19 / ISH_GP1
BE19 GPP_A20 / ISH_GP2
BE18 GPP_A21 / ISH_GP3
BG16 GPP_A22 / ISH_GP4
BE19 GPP_A23 / ISH_GP5

TP51 GPP_B0 — AY22 GPP_B0
TP48 GPP_B1 — AV19 GPP_B1
3VSB R692 10K/4 VRALERT# — BG21 GPP_B2 / VRALERT#
TP54 GPP_B3 — BF21 GPP_B3 / CPU_GP2
VCC3 R693 8.2K1% GPP_B4 — BF22 GPP_B4 / CPU_GP3

BIOS SHOW FAN FAULT Information USE

AR17 GPP_B11
AV22 GPP_B15 / GSPI0_CS#
AY24 GPP_B16 / GSPI0_CLK
BG25 GPP_B17 / GSPI0_MISO
BF25 GPP_B19
BF24 GPP_B20 / GSPI1_CLK
AP24 GPP_B21 / GSPI1_MISO

GPIO

41 PCIE1_16_EN — BA39 GPP_C8 / UART0_RXD
41 PCIE1_8_EN — BG39 GPP_C9 / UART0_TXD
BF39 GPP_C10 / UART0_RTS#
BC45 GPP_C11 / UART0_CTS#
BB45 GPP_C12 / UART1_RXD / ISH_UART1_RXD
BA44 GPP_C13 / UART1_TXD / ISH_UART1_TXD
BA45 GPP_C14 / UART1_RTS# / ISH_UART1_RTS#
BA35 GPP_C15 / UART1_CTS# / ISH_UART1_CTS#

BIOS SHOW FAN MODE Information USE
Default GPI

FAN MODE USE

49 SYSFAN3_MODE — AY44 GPP_C20 / UART2_RXD
49 SYSFAN4_MODE — BA33 GPP_C21 / UART2_TXD
GPP_C22 — AW43 GPP_C22 / UART2_RTS#
USB_SMI_USE
26 GPP_C23_USB3_SMI1 — GPP_C23_USB3_SMI1 — AW42 GPP_C23 / UART2_CTS#

AV41 GPP_D0
AY39 GPP_D1
BB44 GPP_D2
AV43 GPP_D3
AU44 GPP_D4 / ISH_I2C2_SDA / ISH_I2C3_SDA

PCIE1_16_EN R669 100K/4
PCIE1_8_EN R667 100K/4

42 GPP_D4 — GPP_D4
3VSB R580 10K/4 GPP_D9 — AT45 GPP_D9
TP49 GPP_D10 — AV39 GPP_D10
TP46 GPP_D11 — AT38 GPP_D11
TP14 GPP_D12 — AT41 GPP_D12
AP44 GPP_D13 / ISH_UART0_RXD / SML0BDATA / I2C2_SDA
AP43 GPP_D14 / ISH_UART0_TXD / SML0BCLK / I2C2_SCL
AT44 GPP_D15 / ISH_UART0_RTS#
AT39 GPP_D16 / ISH_UART0_CTS#

3VSB
R581 10K/4 GPP_D4
R602 10K/4 GPP_C22
R601 10K/4 GPP_C23_USB3_SMI1

AM44 GPP_D21
AM42 GPP_D22
43 GPPD23_PLTRST# — AN44 GPP_D23 / ISH_I2C2_SCL / ISH_I2C3_SCL

AP17 TP1
AU19 TP2

0825 Add GPPD23_PLTRST# for ASM2142 PLTRST#

PCH_H

VCC3
R939 10K/4 GPPD23_PLTRST#

0825 Add R939 for ASM2142 PLTRST#

GPP_E3 / CPU_GP0 — AP41 GPP_E3 — R561 8.2K1% — VCC3
GPP_E7 / CPU_GP1 — AK43 GPP_E7 — TP44

CPU_SKTOCC# R522 X_10K/4 3VSB

GPP_F14 — AD44 CPU_SKTOCC# — CPU_SKTOCC# 4,42
GPP_F22 — AB45 GPP_F22
GPP_F23 — AE39 GPP_F23 — TP41

GPP_G0 / FAN_TACH_0 — AA43 — PEG_MODE_0 19
GPP_G1 / FAN_TACH_1 — AB44 — PEG_MODE_1 19
GPP_G2 / FAN_TACH_2 — AC36 — XMP_LED 50
GPP_G3 / FAN_TACH_3 — T44
GPP_G4 / FAN_TACH_4 — AC33
GPP_G5 / FAN_TACH_5 — V43 — BIOS_SEL_PCIESATA2 25
GPP_G6 / FAN_TACH_6 — Y42 — M2_2_SEL 23,25
GPP_G7 / FAN_TACH_7 — AA44 — BIOS_DIS_SW2 25
GPP_G8 / FAN_PWM_0 — W44
GPP_G9 / FAN_PWM_1 — Y44
GPP_G10 / FAN_PWM_2 — AC35
GPP_G11 / FAN_PWM_3 — AC41
GPP_G12 / GSXDOUT — AC39
GPP_G13 / GSXSLOAD — Y36
GPP_G14 / GSXDIN — Y43
GPP_G15 / GSXSRESET# — U44
GPP_G16 / GSXCLK — T43
GPP_G17 / ADR_COMPLETE — V42
GPP_G18 / NMI# — U45 NMI# — R502 10K/4 — 3VSB
GPP_G19 / SMI# — R43 SMI# — R500 10K/4 — 3VSB
GPP_G20 — Y35 TEST_SETUP_MENU — R504 10K/4 — VCC3
GPP_G21 — AC30 GPP_G21 — R506 X_10K/4 — 3VSB
GPP_G22 — R45 GPP_G22
GPP_G23 — R44 GPP_G23

CPU X16/X8 SEL GPIO

GPP_F22 R516 10K/4
PEG_MODE_1 R517 10K/4 — 3VSB
PEG_MODE_0 R515 10K/4
XMP_LED R306 10K/4

For BIOS BOM USE
R582 10K/4 GPP_G21 — R562 X_10K/4
R501 10K/4 GPP_G22 — R492 X_10K/4
R503 10K/4 GPP_G23 — R505 X_10K/4 — 3VSB

GPD7 / RSVD — BG11 GPD7 — TP17

RSVD-0 V11
RSVD-1 V13
RSVD-2 AC13
RSVD-3 AF17
RSVD-4 AG17
RSVD-5 AH14
RSVD-6 AH16
RSVD-7 M33
RSVD-8 N33
RSVD-9 AU22
RSVD-10 P27
RSVD-11 T27
RSVD-12 T33
RSVD-13 T35
RSVD-14 N29
RSVD-15 P29
RSVD-16 T24
RSVD-17 P24
RSVD-18 AP29 — TP_EDM — R913 1K/4
RSVD-19 BF1
RSVD-20 BG2

CRB0.7

MICRO-STAR INT'L CO.,LTD		
MS-7A63		
Size: Custom	Document Description: PCH-LPC/SPI/SMBUS/MISC	Rev: 10
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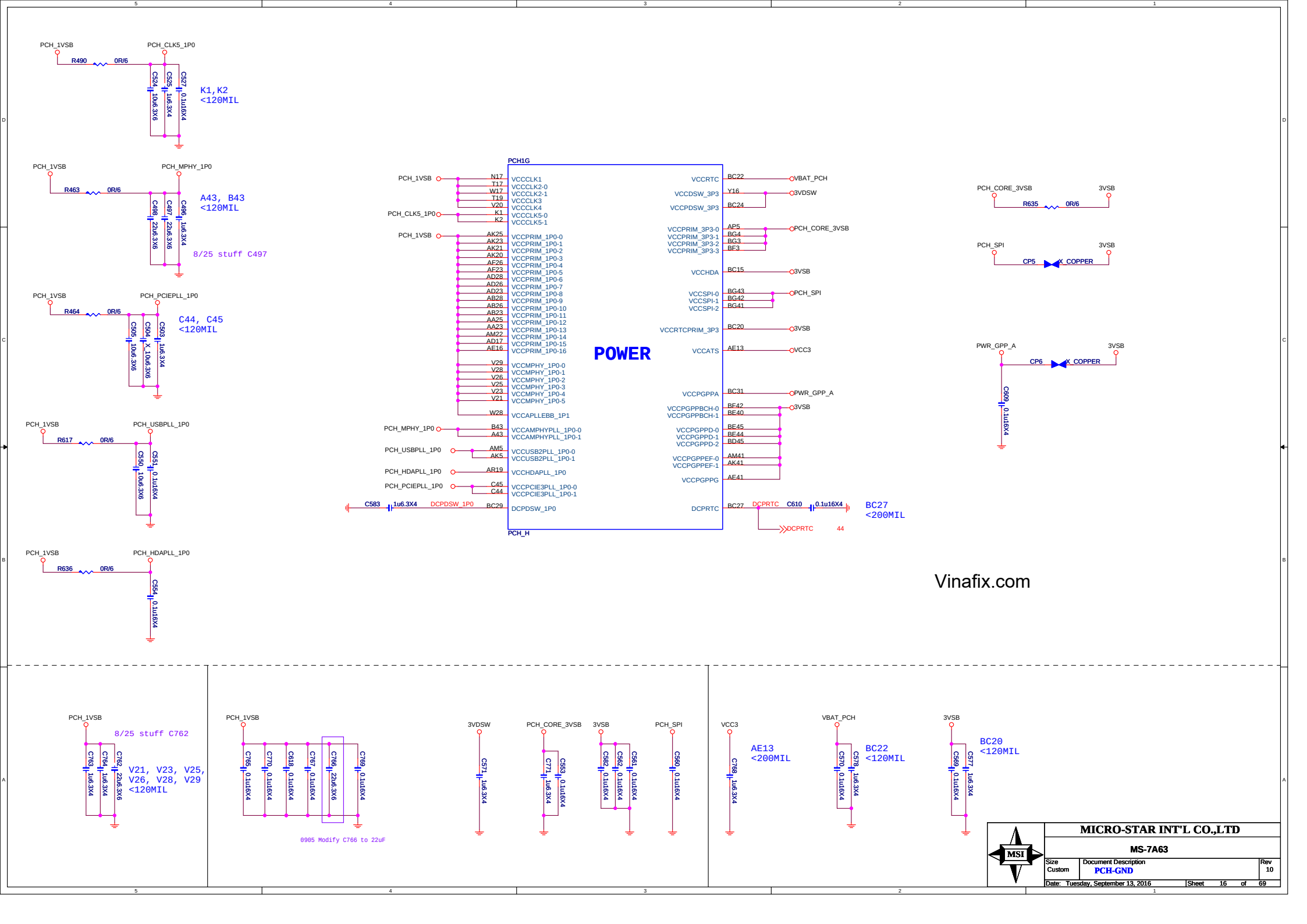
PCH_1VSB
R490 0R/6
PCH_CLK5_1P0
C524 10u6.3X6
C525 1u6.3X4
C527 0.1u16X4
K1,K2
<120MIL
PCH_1VSB
R463 0R/6
PCH_MPHY_1P0
C498 22u6.3X6
C497 22u6.3X6
C496 1u6.3X4
A43, B43
<120MIL
8/25 stuff C497
PCH_1VSB
R464 0R/6
PCH_PCIEPLL_1P0
C505 10u6.3X6
C504 X_10u6.3X6
C503 1u6.3X4
C44, C45
<120MIL
PCH_1VSB
R617 0R/6
PCH_USBPLL_1P0
C550 10u6.3X6
C551 0.1u16X4
PCH_1VSB
R636 0R/6
PCH_HDAPLL_1P0
C554 0.1u16X4
PCH1G
PCH_1VSB
N17 VCCCLK1
T17 VCCCLK2-0
W17 VCCCLK2-1
T19 VCCCLK3
V20 VCCCLK4
PCH_CLK5_1P0
K1 VCCCLK5-0
K2 VCCCLK5-1
PCH_1VSB
AK25 VCCPRIM_1P0-0
AK23 VCCPRIM_1P0-1
AK21 VCCPRIM_1P0-2
AK20 VCCPRIM_1P0-3
AF26 VCCPRIM_1P0-4
AF23 VCCPRIM_1P0-5
AD28 VCCPRIM_1P0-6
AD26 VCCPRIM_1P0-7
AD23 VCCPRIM_1P0-8
AB28 VCCPRIM_1P0-9
AB26 VCCPRIM_1P0-10
AB23 VCCPRIM_1P0-11
AA25 VCCPRIM_1P0-12
AA23 VCCPRIM_1P0-13
AM22 VCCPRIM_1P0-14
AD17 VCCPRIM_1P0-15
AE16 VCCPRIM_1P0-16
V29 VCCMPHY_1P0-0
V28 VCCMPHY_1P0-1
V26 VCCMPHY_1P0-2
V25 VCCMPHY_1P0-3
V23 VCCMPHY_1P0-4
V21 VCCMPHY_1P0-5
W28 VCCAPLLEBB_1P1
PCH_MPHY_1P0
B43 VCCAMPHYPLL_1P0-0
A43 VCCAMPHYPLL_1P0-1
PCH_USBPLL_1P0
AM5 VCCUSB2PLL_1P0-0
AK5 VCCUSB2PLL_1P0-1
PCH_HDAPLL_1P0
AR19 VCCHDAPLL_1P0
PCH_PCIEPLL_1P0
C45 VCCPCIE3PLL_1P0-0
C44 VCCPCIE3PLL_1P0-1
C583 1u6.3X4 DCPDSW_1P0
BC29 DCPDSW_1P0
POWER
PCH_H
VCCRTC BC22 VBAT_PCH
VCCDSW_3P3 Y16 3VDSW
VCCPDSW_3P3 BC24
VCCPRIM_3P3-0 AP5
VCCPRIM_3P3-1 BG4
VCCPRIM_3P3-2 BG3
VCCPRIM_3P3-3 BF3
PCH_CORE_3VSB
VCCHDA BC15 3VSB
VCCSPI-0 BG43
VCCSPI-1 BG42
VCCSPI-2 BG41
PCH_SPI
VCCRTCPRIM_3P3 BC20 3VSB
VCCATS AE13 VCC3
VCCPGPPA BC31 PWR_GPP_A
VCCPGPPBCH-0 BF42
VCCPGPPBCH-1 BE40
3VSB
VCCPGPPD-0 BE45
VCCPGPPD-1 BE44
VCCPGPPD-2 BD45
VCCPGPPEF-0 AM41
VCCPGPPEF-1 AK41
VCCPGPPG AE41
DCPRTC BC27 DCPRTC C610 0.1u16X4
DCPRTC 44
BC27
<200MIL
PCH_CORE_3VSB
R635 0R/6
3VSB
PCH_SPI
CP5 X_COPPER
3VSB
PWR_GPP_A
CP6 X_COPPER
3VSB
C609 0.1u16X4
Vinafix.com
PCH_1VSB
8/25 stuff C762
C763 1u6.3X4
C764 1u6.3X4
C762 22u6.3X6
V21, V23, V25,
V26, V28, V29
<120MIL
PCH_1VSB
C765 0.1u16X4
C770 0.1u16X4
C618 0.1u16X4
C767 0.1u16X4
C766 22u6.3X6
C769 0.1u16X4
0905 Modify C766 to 22uF
3VDSW
C571 1u6.3X4
PCH_CORE_3VSB
C771 1u6.3X4
C553 0.1u16X4
3VSB
C582 0.1u16X4
C562 0.1u16X4
C561 0.1u16X4
PCH_SPI
C560 0.1u16X4
VCC3
C768 1u6.3X4
AE13
<200MIL
VBAT_PCH
C570 0.1u16X4
C578 1u6.3X4
BC22
<120MIL
3VSB
C569 0.1u16X4
C577 1u6.3X4
BC20
<120MIL
MSI
MICRO-STAR INT'L CO.,LTD
MS-7A63
Size Custom
Document Description PCH-GND
Rev 10
Date: Tuesday, September 13, 2016
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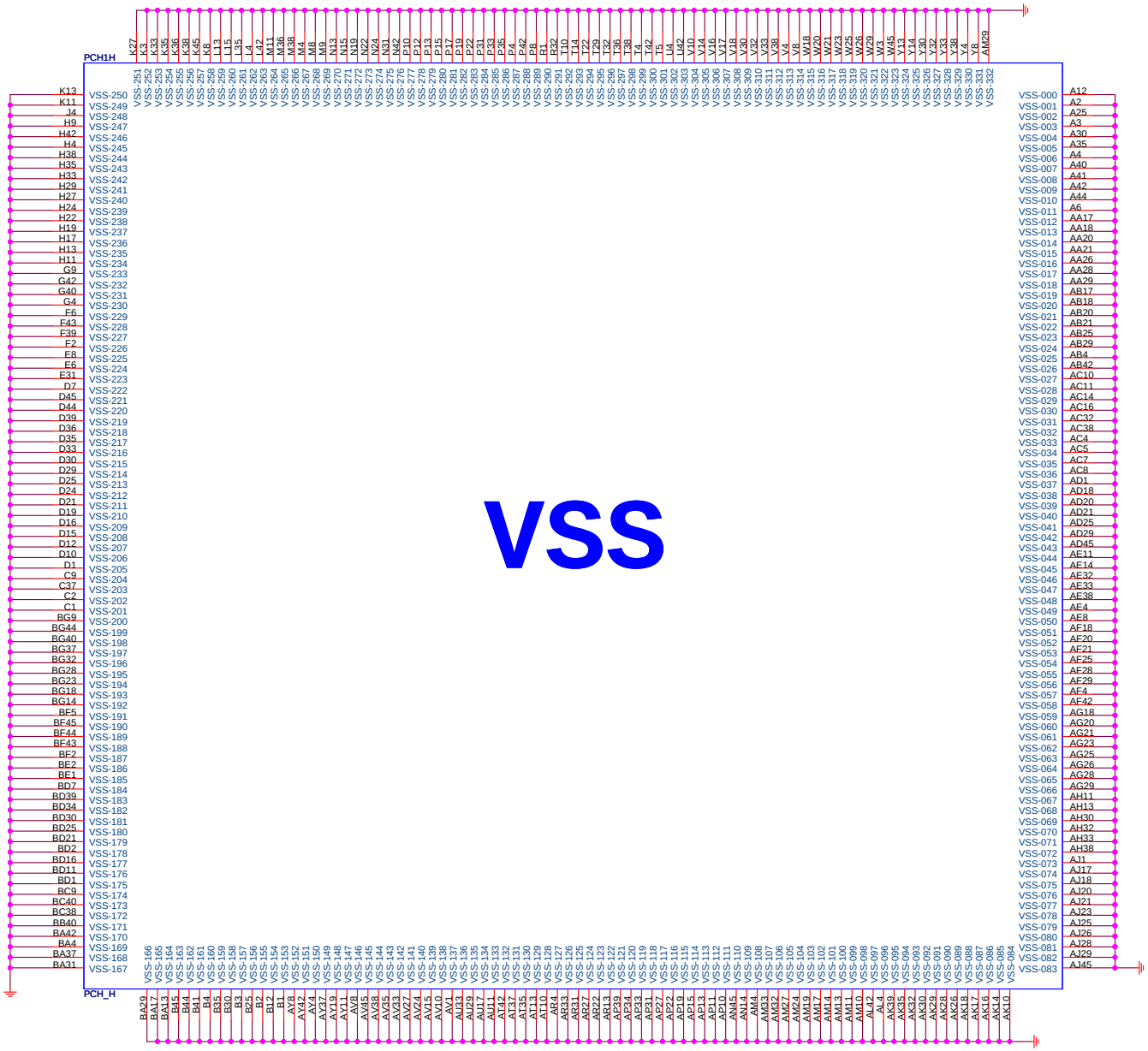

MICRO-STAR INT'L CO.,LTD		
MS-7A63		
Size: Custom	Document Description: PCH-Power	Rev: 10
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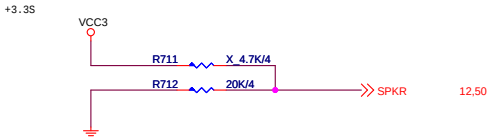
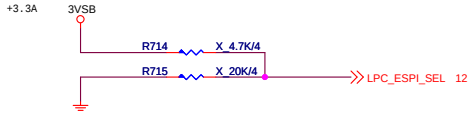
TOP Swap



Internal pull-down is disabled after PLTRST#

LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

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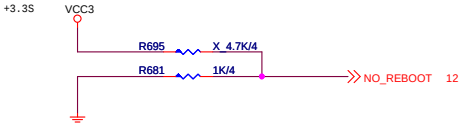
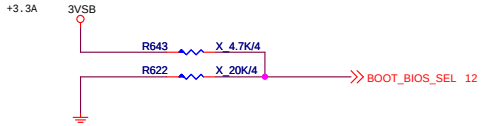
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

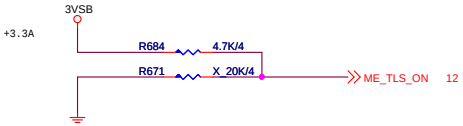
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

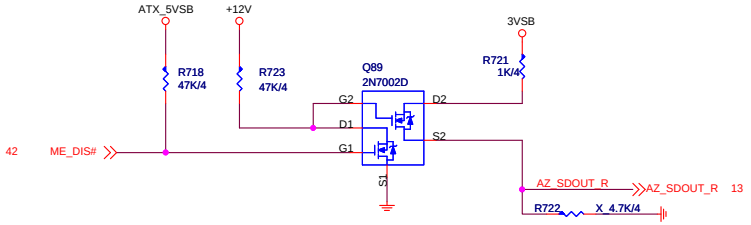
AMT and SBA with confidentiality



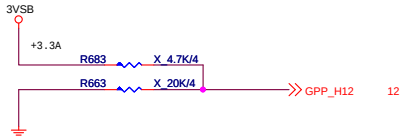
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA_SDO



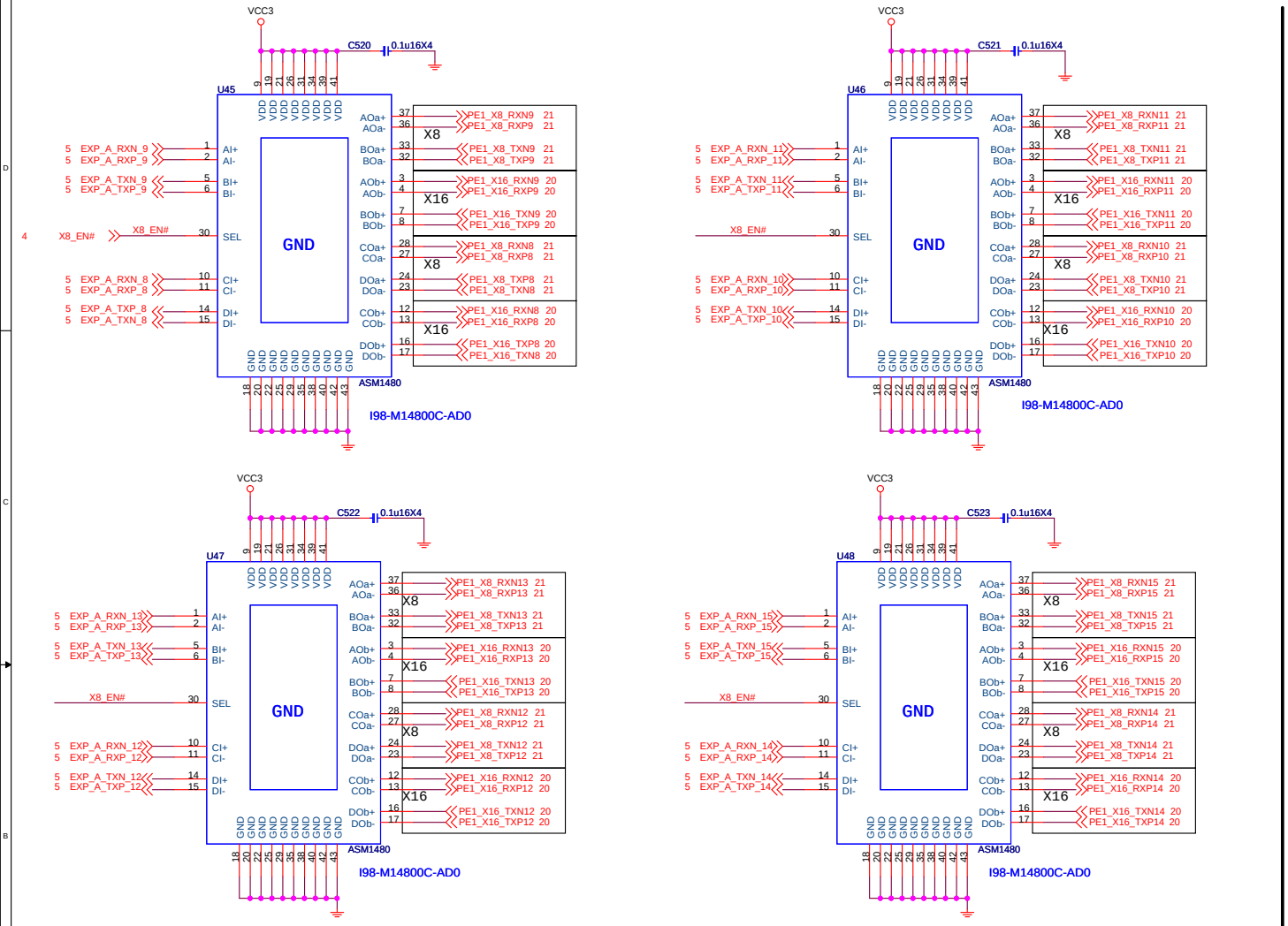
ESPI FLASH SHARING MODE

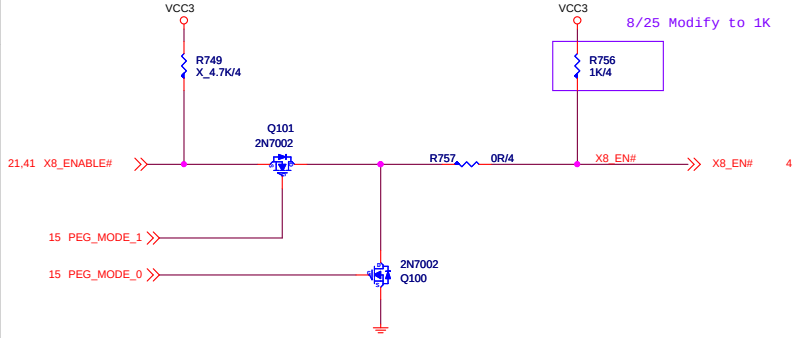


0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down is disabled after RSMRST

MICRO-STAR INT'L CO.,LTD		
MS-7A63		
Size: Custom	Document Description: PCH-Strap	Rev: 10
Date: Tuesday, September 13, 2016	Sheet 18 of 69	





MODE_1

0: BIOS MODE
1: HW MODE (Default)

HW MODE

PCH Status	MODE_0	MODE_1
AUTO	0	1

If USE HW MODE
GPP_G0 & GPP_G1 programming to GPI

If USE BIOS MODE
GPP_G0 & GPP_G1 programming to GPO

BIOS MODE

PCH Status	MODE_0	MODE_1
16,0	0	0
8,8	1	0

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	PCIE SWITCH	10

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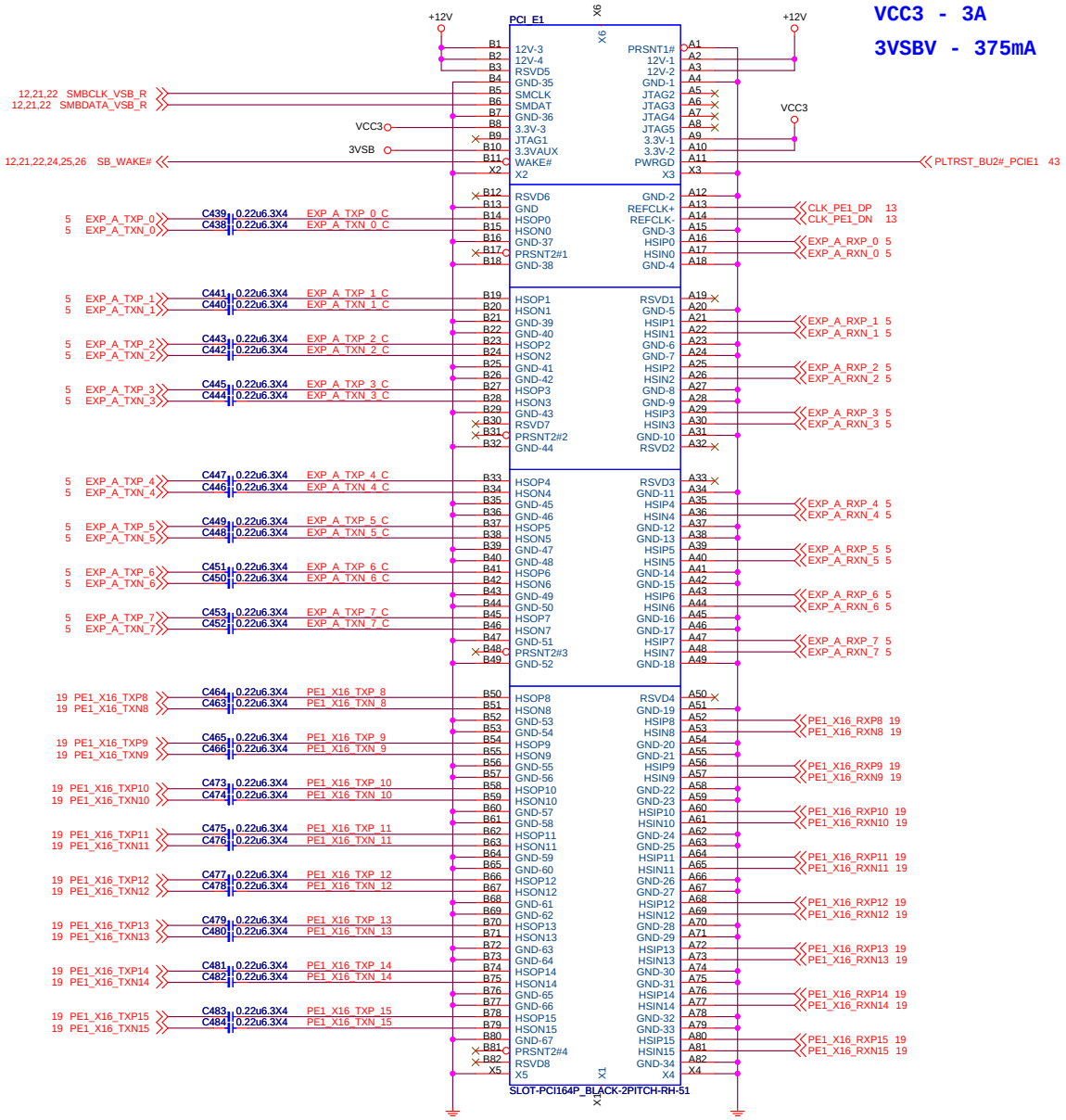
12V - 5.5A

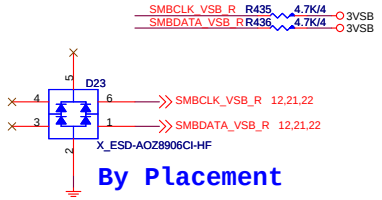
VCC3 - 3A

3VSBV - 375mA



0901 Modify PCI_E1 PIN X2.X3.X4.X5 Connect to GND

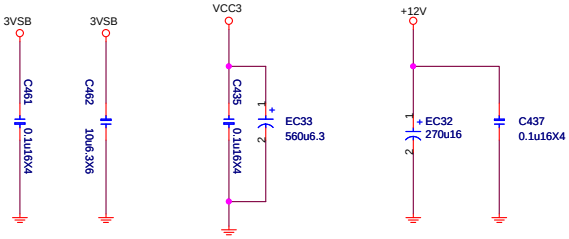
SMBUS ESD



By Placement

Main:D0G-05A0529-A68

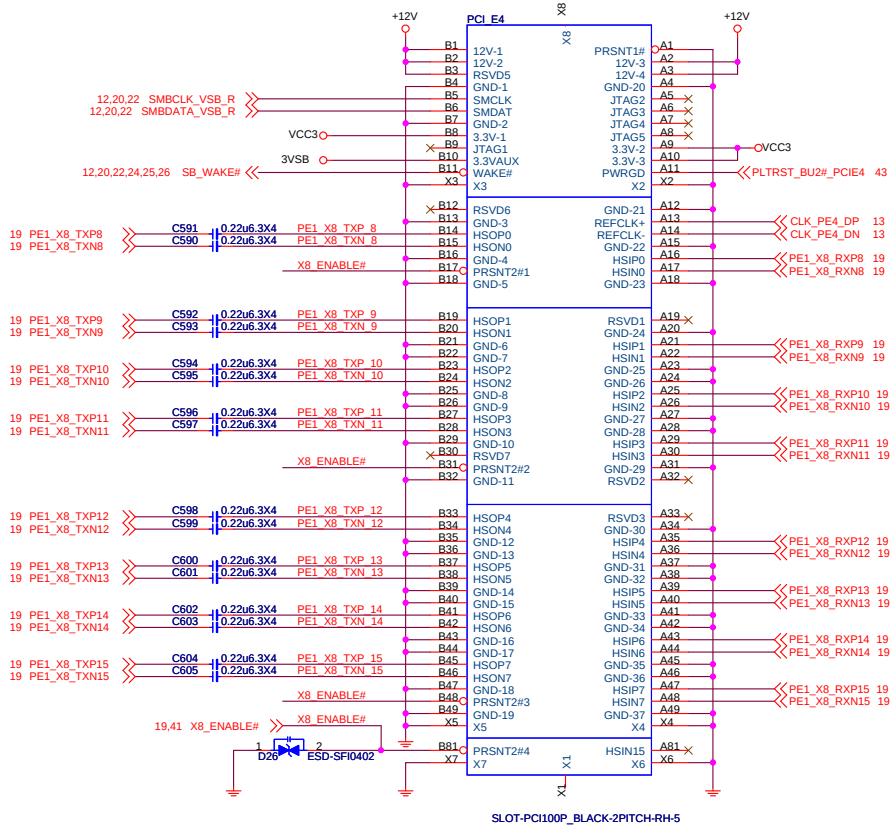
AVL:D0G-45B0510-I14

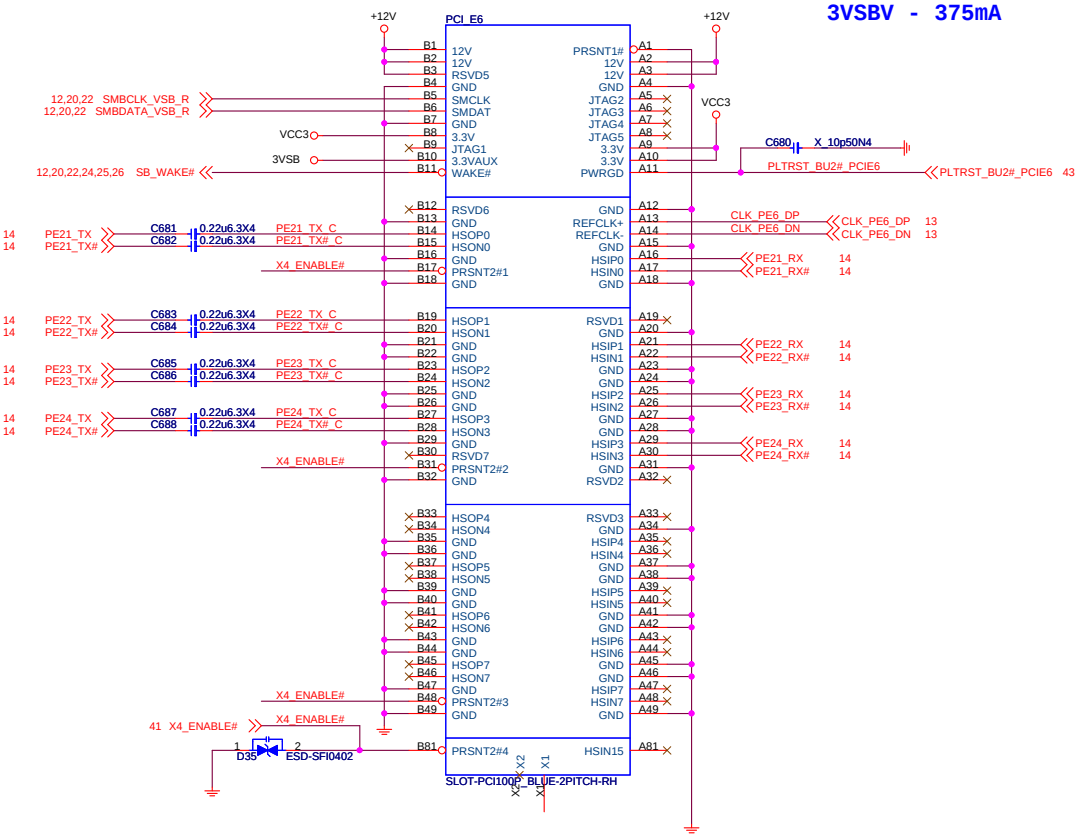


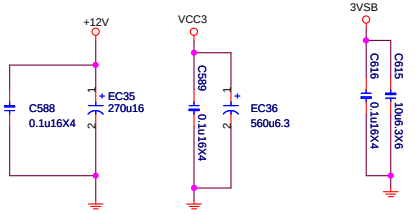
MICRO-STAR INT'L CO.,LTD	
MS-7A63	
Size: Custom	Document Description: PCIE SLOT (X16)
Rev: 10	
Date: Tuesday, September 13, 2016	Sheet 20 of 69

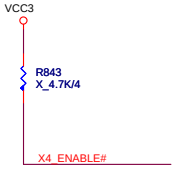
PCI_Express X4 Slot

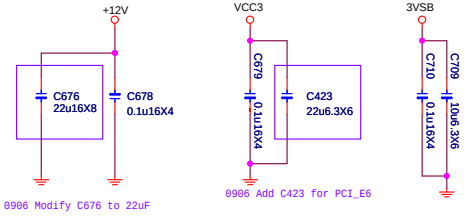
12V - 2.1A
VCC3 - 3A
3VSBV - 375mA











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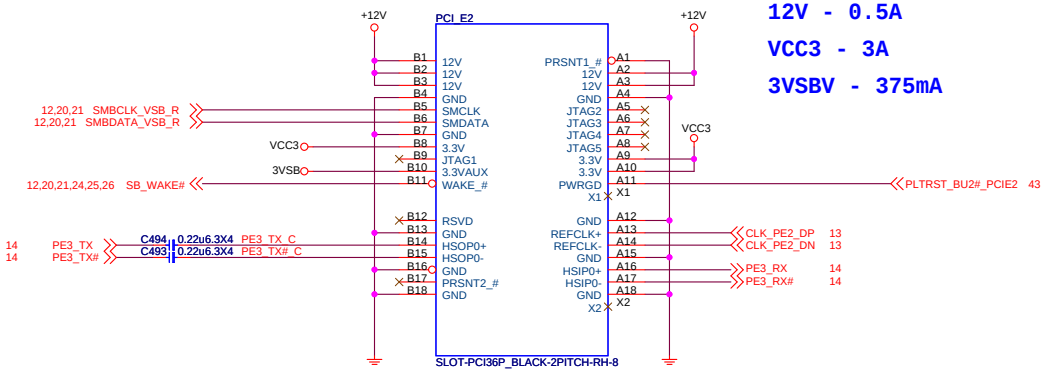
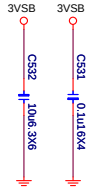
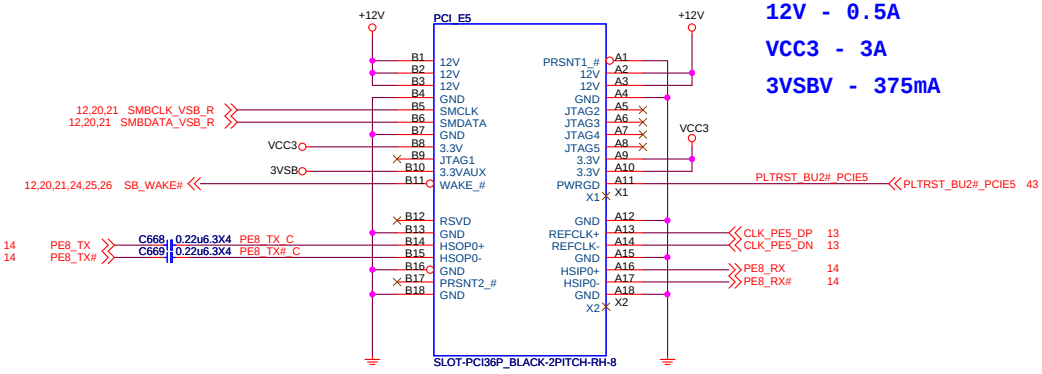
MICRO-STAR INT'L CO.,LTD		
MS-7A63		
Size: Custom	Document Description: PCIE SLOT (X4)	Rev: 10
Date: Tuesday, September 13, 2016	Sheet 21 of 69	

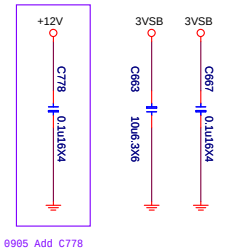
2016.08.25 Modify to N11-0360211-F02



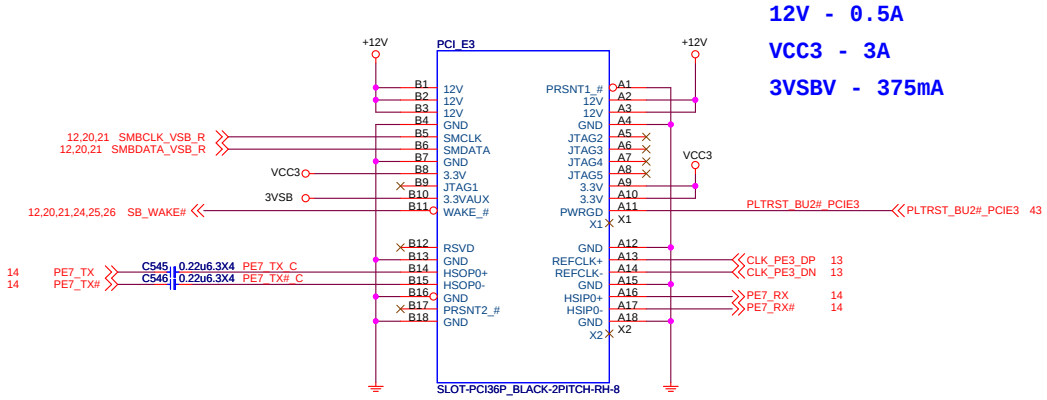


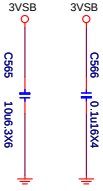
2016.08.25 Modify to N11-0360211-F02





2016.08.25 Modify to N11-0360211-F02





MICRO-STAR INT'L CO.,LTD

MS-7A63

Size	Document Description	Rev
Custom	PCIE SLOT (X1)	10

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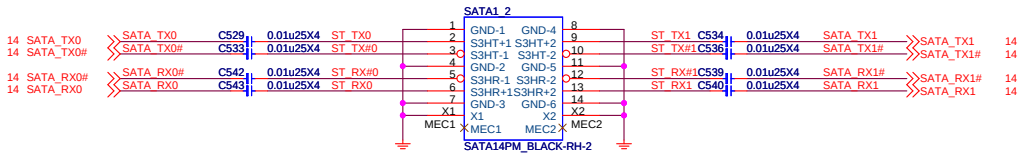

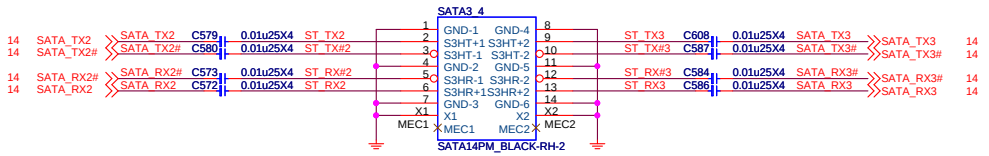

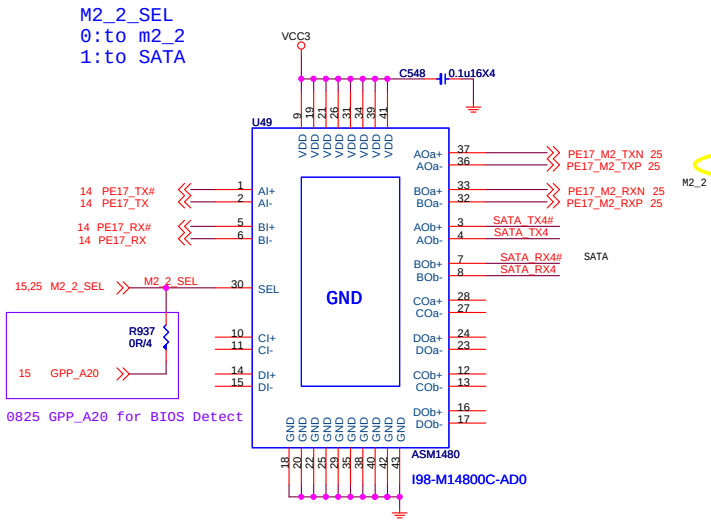

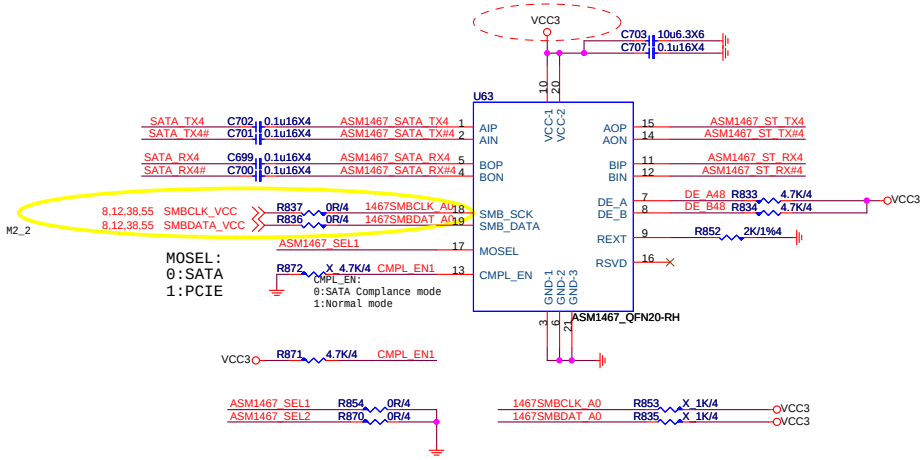

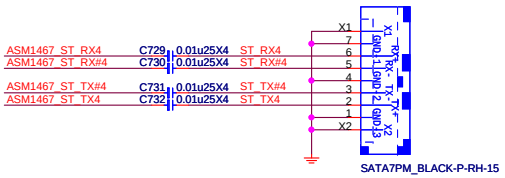

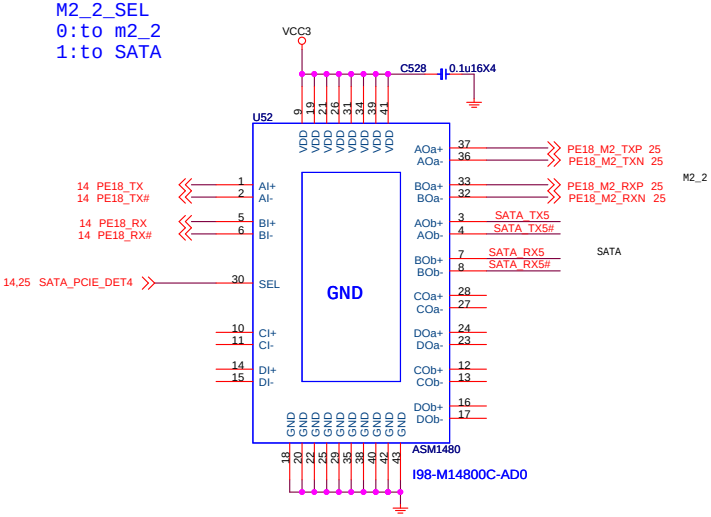

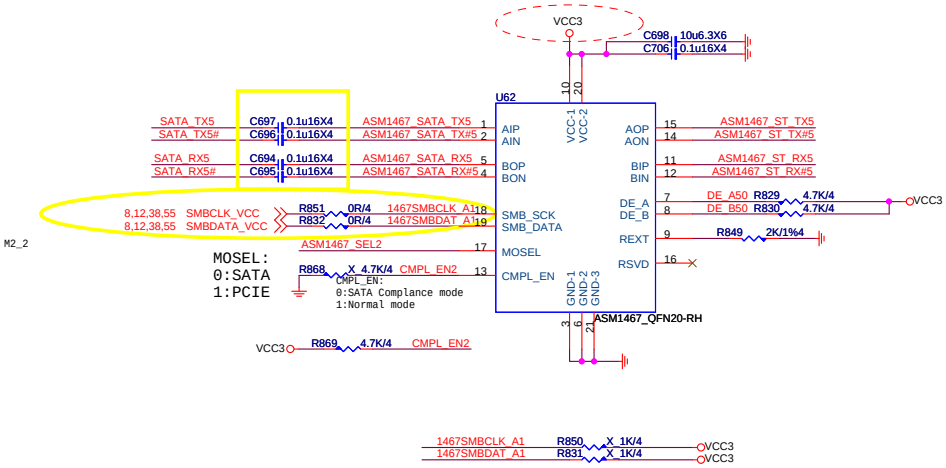

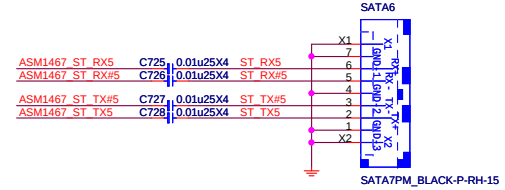

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MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	SATA Connector	10

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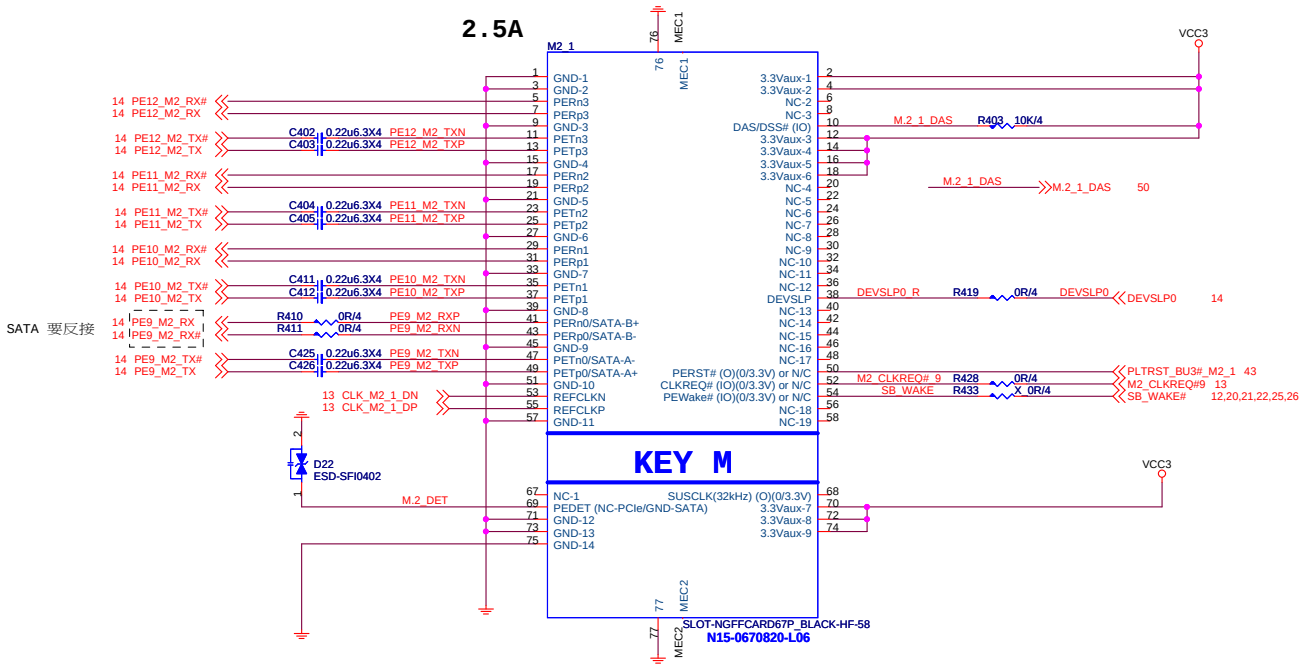
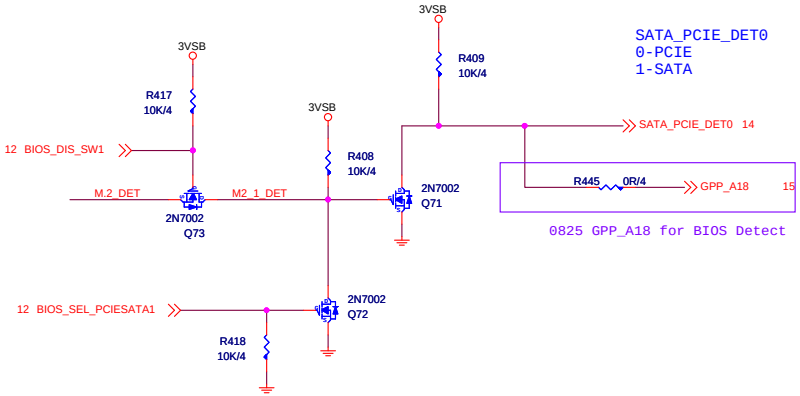


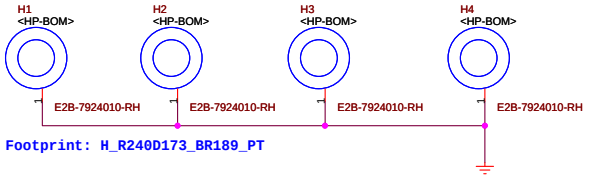


SATA_PCIE_DET0
0-PCIE
1-SATA

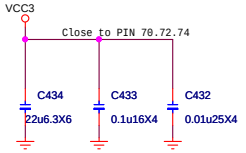
0825 GPP_A18 for BIOS Detect

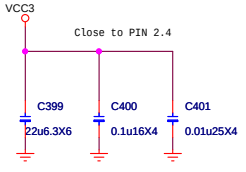
BIOS_MODE

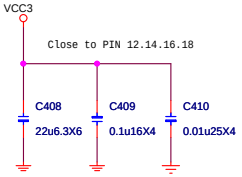
	GPP_H15	GPP_H13
BIOS_DIS_SW1	***BIOS_SEL_PCIESATA1***	***Mode***
0	***1***	***M2-SATA***
0	***0***	***M2-PCIE***
GPI	***GPI***	***AUTO***



Footprint: H_R240D173_BR189_PT







MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	M.2-SLOT1	10

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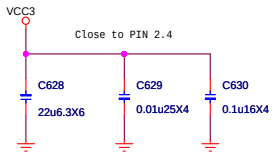
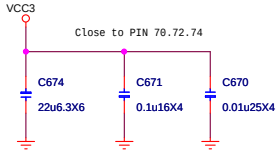
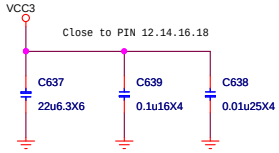
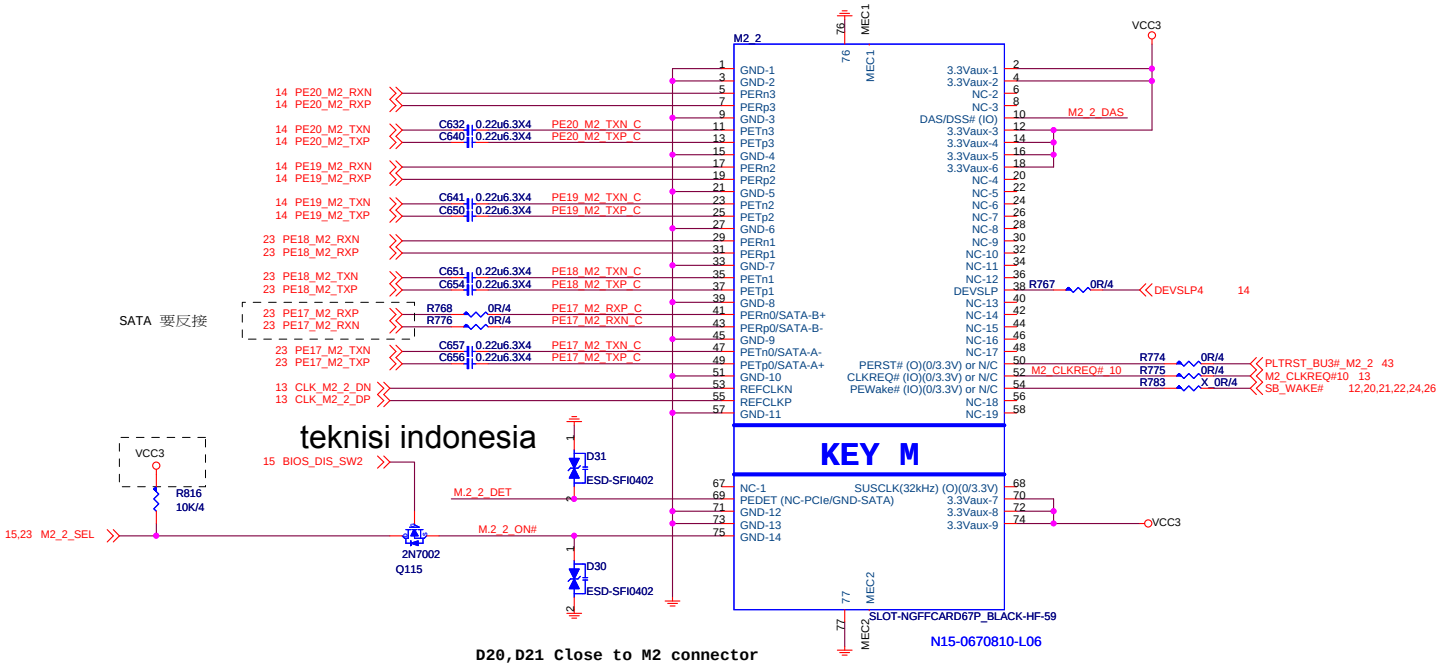
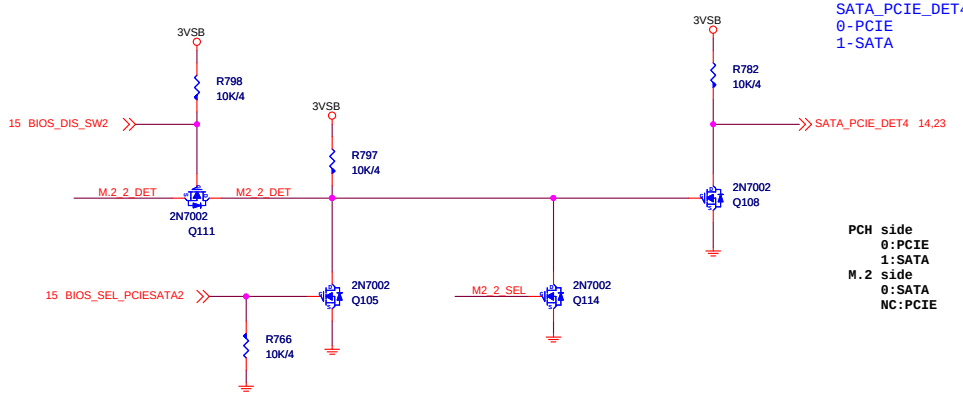


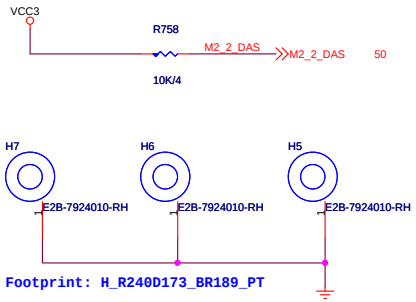






D20,D21 Close to M2 connector





BIOS_MODE

GPP_G7 GPP_G6 GPP_G5

BIOS_DIS_SW	*M2_2_SEL*	*BIOS_SEL_PCIESATA2*	*Mode*
GPI(1)	*GPI(1)*	*GPI(0)*	*AUTO*
0	*1*	*0*	*SATA5*
0	*0*	*1*	*M2-SATA*
0	*0*	*0*	*M2-PCIE*

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	M.2-SLOT2	10

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Minimun gap should be greater of
>15mil with other signal.

USB HS (90Ohm-Diff)

Chip to Connector ¯1.5 inch.

Power Consumption

	3.3V	1.2V(1.05V	3.3VSUS	1.05VSUS(1.2VSUS	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA		1573.8(mW)
ASM2142	TDP	TDP	TDP	TDP	300mA(TDP)	TDP

Layout Guide:

1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2

CLK Rule (Follow SB PDG)

PCIE Rule (Follow SB PDG)

UU5A 1042 ASM1142

ASM1142 RU16 stuff RU17 unstuff
ASM2142 RU16 unstuff RU17 stuff

0909 Modify to ASM2142

UU5B 1042 ASM1142

ASM1142-RH-3

SMI connect to GPI which
support smi function.
SB side pull high 10K ohm to 3VSB.
(Intel 8X & 9X series use GPIO10)
(Intel SKL use GPP_C23)

PPON_X Internal Pull-up to VCC3

OCI_X Internal Pull-up to SUS

RX/TX Internal Pull-up

1.0->ASM2142 (B02-021420C-AD0)

B02-021421C-AD0

YU1
D04-0900900-SC6(M)
D04-0901200-F07
D04-0901100-T16

X0/XI (95hm-Diff,Spacing 30mil)
UREXT,PEUREXT(W/S) : 10/7
OCIA,OCIB,PPONA,PPONB(W/S) : 5/8

ASM1142 RU19 stuff RU18 unstuff
ASM2142 RU19 unstuff RU18 stuff

teknisi indonesia

atx5vsb change to vcc5

ASM_SMI has internal Pull-up to VCC
ASM_WAKE has internal Pull-up to VCCSUS

ASM1142 1.2 VCC Power

SN:L01-0107118-M26

0826 Add CU41&L23 for USB3_1P2

MP2143DJ_TSOT23-8-RH

0909 Modify to ASM2142

ASM1142 RU13/RU14 200K/187K__1.24V
ASM2142 RU13/RU14 196K/261K__1.05V

UU2 GS7116S5-ADJ-R

ASM1142 unstuff
ASM2142 stuff

ASM1142 1.2 VSB Power

UU1 GS7116S5-ADJ-R

ASM1142 RU9 18K__1.2V
ASM2142 RU9 31.6K__1.05V 0909 Modify to ASM2142

EEPROM

UU3 MX25L512EMI-10G

M31-25L1022-M24

ASM1142 UU3 M31-2551222-M24(512K bit)
ASM2142 UU3 M31-25L1022-M24(1M bit)

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	ASM 1142	10

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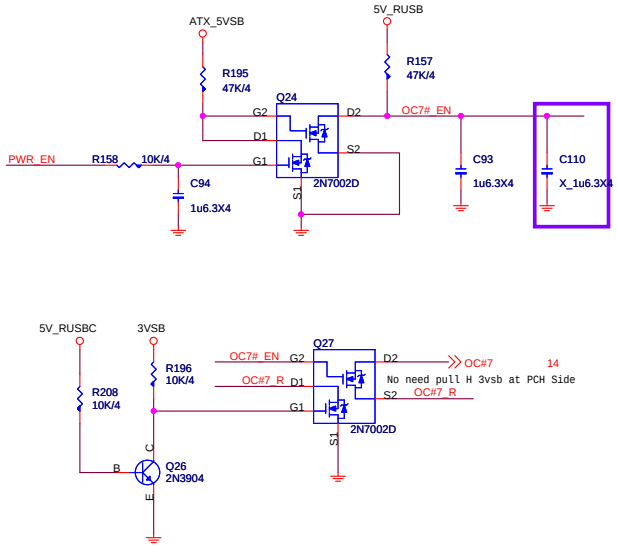
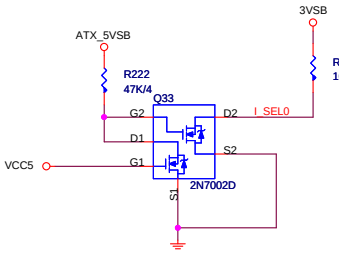
VBUS OC#



Current Mode

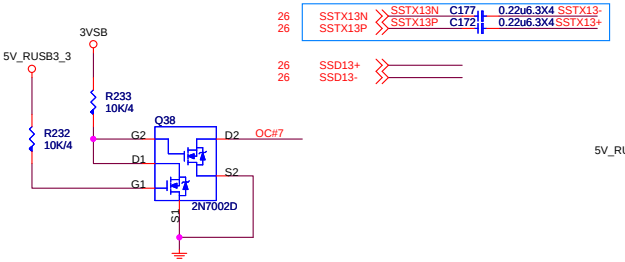


I_SEL0 : I_SEL1

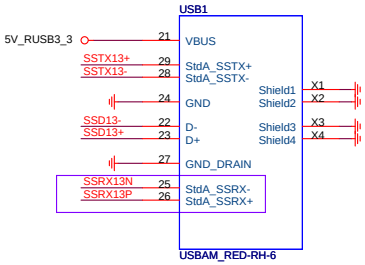
X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

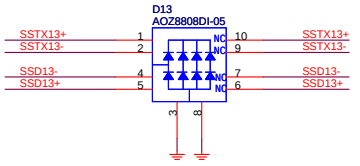
1.5A under S3 mode
3A under S0 mode

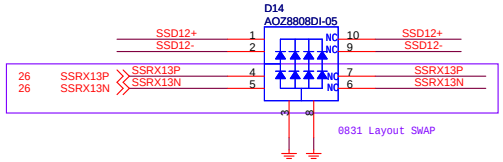
TYPE-A

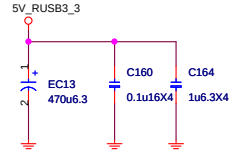


2016.08.24 Modify to N53-09M0861-L06

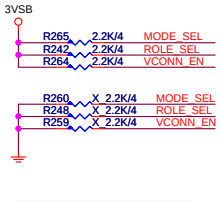








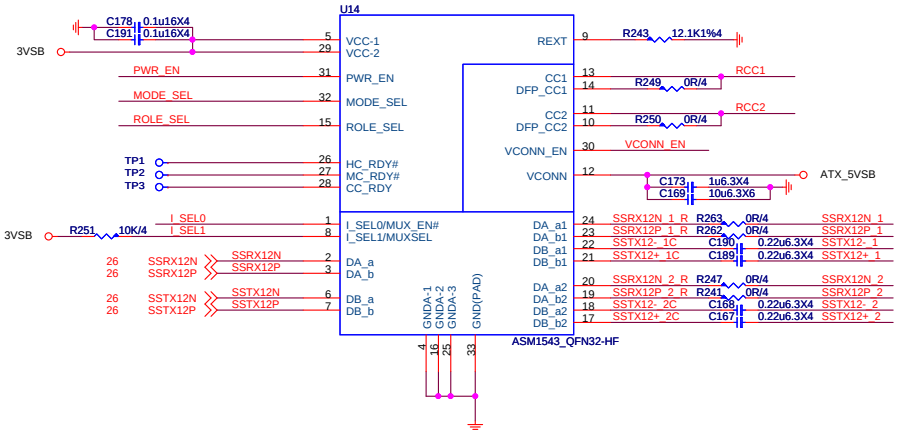
USB Type-C MUX with Configuration Channel (CC)

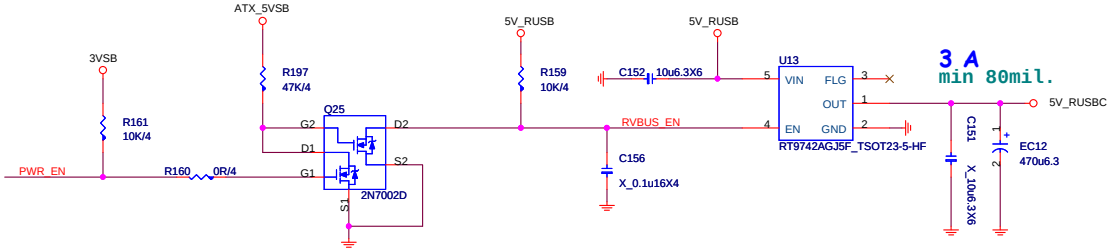


MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

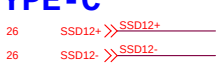
ROLE_SEL	
1	DFP role (default)
0	UFP role

VCONN_EN	
1	enable
0	disable

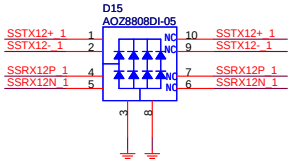


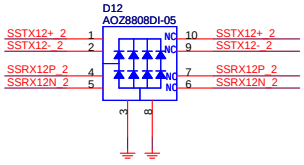


TYPE-C



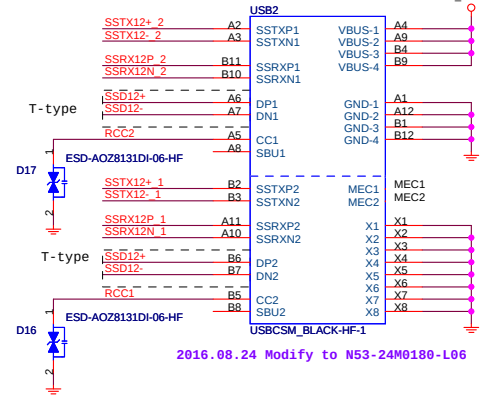
OC#7





ESD Protection
NEAR CONNECTOR

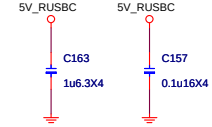
USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-005 AVL



2016.08.24 Modify to N53-24M0180-L06

D16.D17
D0G-12A060C-A68 Main
D0G-0600600-I05 AVL
D0G-0500600-L07 AVL

close to Type C Connector



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MS-7A63		
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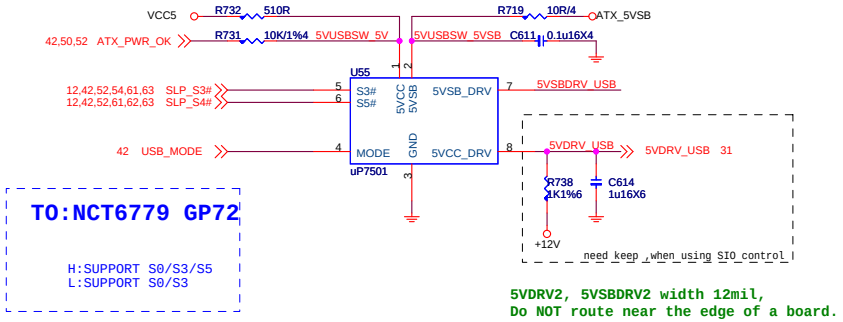
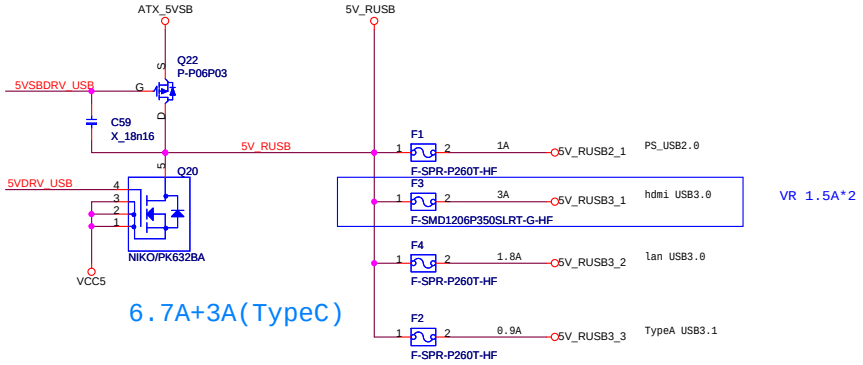
USB PORT POWER



5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.

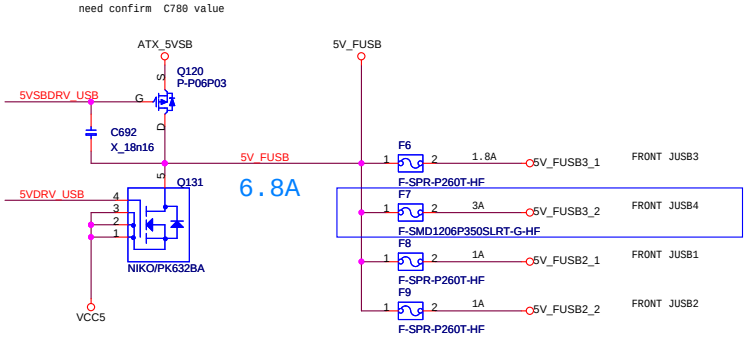
REAR USB PORT POWER



6.7A+3A(TypeC)

VR 1.5A*2

FRONT USB PORT POWER



6.8A

VR 1.5A*2

P-MOS
D03-06P0319-N03

N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

D08-0301000-P16
D08-0301100-B07

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MS-7A63		
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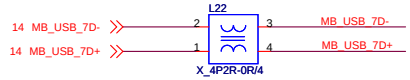
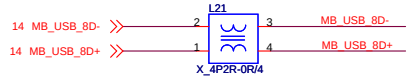
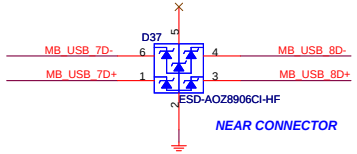
Date: Tuesday, September 13, 2016	Sheet 28 of 69	

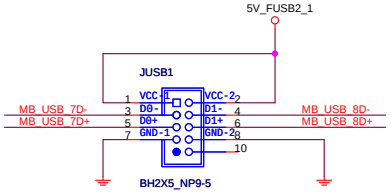




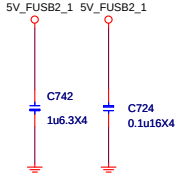


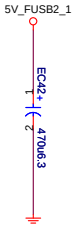
Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14

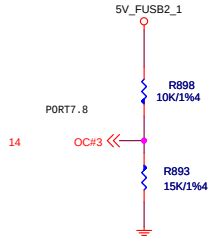
1.0A

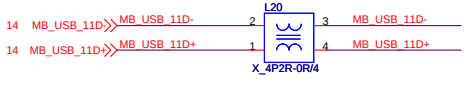


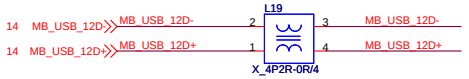
EMI Cap near Connector.

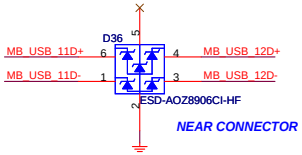






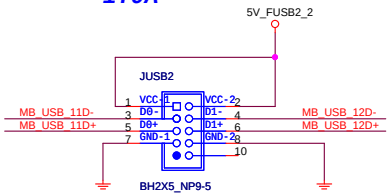




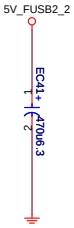


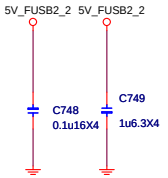
Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14

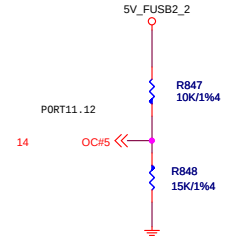
1.0A



EMI Cap near Connector.







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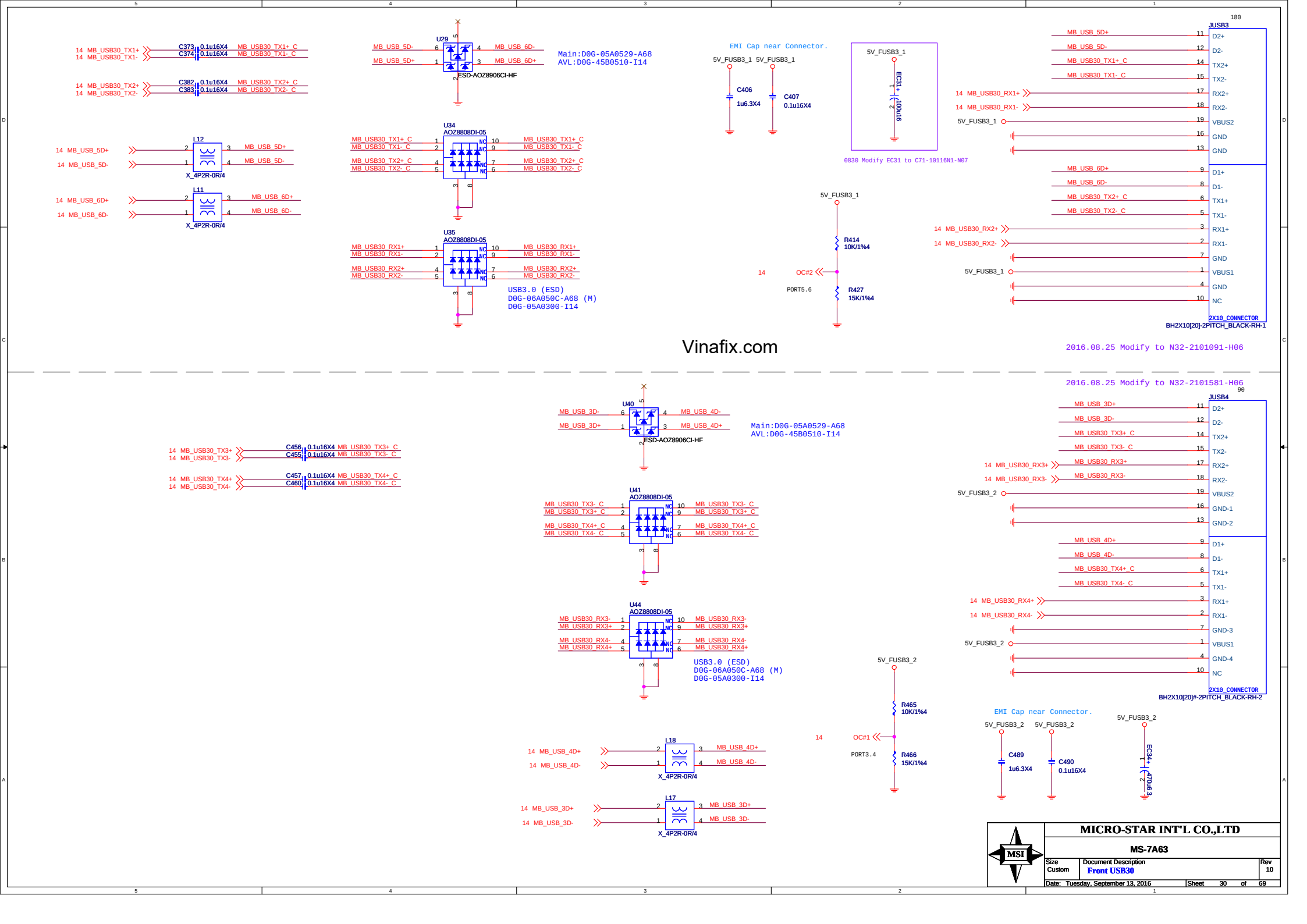
14 MB_USB30_TX1+
14 MB_USB30_TX1-
C373 0.1u16X4 MB_USB30_TX1+_C
C374 0.1u16X4 MB_USB30_TX1-_C
14 MB_USB30_TX2+
14 MB_USB30_TX2-
C382 0.1u16X4 MB_USB30_TX2+_C
C383 0.1u16X4 MB_USB30_TX2-_C
U29
MB_USB_5D-
MB_USB_5D+
MB_USB_6D-
MB_USB_6D+
ESD-AOZ8906CI-HF
Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14
EMI Cap near Connector.
5V_FUSB3_1
C406 1u6.3X4
C407 0.1u16X4
EC31 100u16
0830 Modify EC31 to C71-10116N1-N07
JUSB3
MB_USB_5D+
MB_USB_5D-
MB_USB30_TX1+_C
MB_USB30_TX1-_C
14 MB_USB30_RX1+
14 MB_USB30_RX1-
5V_FUSB3_1
D2+
D2-
TX2+
TX2-
RX2+
RX2-
VBUS2
GND
NC
D1+
D1-
TX1+
TX1-
RX1+
RX1-
VBUS1
2X10_CONNECTOR
BH2X10[20]-2PITCH_BLACK-RH-1
L12
L11
X_4P2R-0R/4
U34
AOZ8808DI-05
MB_USB30_TX1+_C
MB_USB30_TX1-_C
MB_USB30_TX2+_C
MB_USB30_TX2-_C
U35
MB_USB30_RX1+
MB_USB30_RX1-
MB_USB30_RX2+
MB_USB30_RX2-
USB3.0 (ESD)
D0G-06A050C-A68 (M)
D0G-05A0300-I14
R414 10K/1%4
R427 15K/1%4
14 OC#2
PORT5.6
MB_USB_6D+
MB_USB_6D-
MB_USB30_TX2+_C
MB_USB30_TX2-_C
14 MB_USB30_RX2+
14 MB_USB30_RX2-
2016.08.25 Modify to N32-2101091-H06
Vinafix.com
14 MB_USB30_TX3+
14 MB_USB30_TX3-
C456 0.1u16X4 MB_USB30_TX3+_C
C455 0.1u16X4 MB_USB30_TX3-_C
14 MB_USB30_TX4+
14 MB_USB30_TX4-
C457 0.1u16X4 MB_USB30_TX4+_C
C460 0.1u16X4 MB_USB30_TX4-_C
U40
MB_USB_3D-
MB_USB_3D+
MB_USB_4D-
MB_USB_4D+
ESD-AOZ8906CI-HF
Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14
U41
AOZ8808DI-05
MB_USB30_TX3-_C
MB_USB30_TX3+_C
MB_USB30_TX4+_C
MB_USB30_TX4-_C
U44
AOZ8808DI-05
MB_USB30_RX3-
MB_USB30_RX3+
MB_USB30_RX4-
MB_USB30_RX4+
USB3.0 (ESD)
D0G-06A050C-A68 (M)
D0G-05A0300-I14
2016.08.25 Modify to N32-2101581-H06
JUSB4
MB_USB_3D+
MB_USB_3D-
MB_USB30_TX3+_C
MB_USB30_TX3-_C
14 MB_USB30_RX3+
14 MB_USB30_RX3-
5V_FUSB3_2
D2+
D2-
TX2+
TX2-
RX2+
RX2-
VBUS2
GND-1
GND-2
MB_USB_4D+
MB_USB_4D-
MB_USB30_TX4+_C
MB_USB30_TX4-_C
14 MB_USB30_RX4+
14 MB_USB30_RX4-
5V_FUSB3_2
D1+
D1-
TX1+
TX1-
RX1+
RX1-
GND-3
VBUS1
GND-4
NC
2X10_CONNECTOR
BH2X10[20]#-2PITCH_BLACK-RH-2
L18
L17
X_4P2R-0R/4
14 MB_USB_4D+
14 MB_USB_4D-
14 MB_USB_3D+
14 MB_USB_3D-
R465 10K/1%4
R466 15K/1%4
14 OC#1
PORT3.4
EMI Cap near Connector.
C489 1u6.3X4
C490 0.1u16X4
EC34 470u6.3
MICRO-STAR INT'L CO.,LTD
MS-7A63
Size Custom
Document Description
Front USB30
Rev 10
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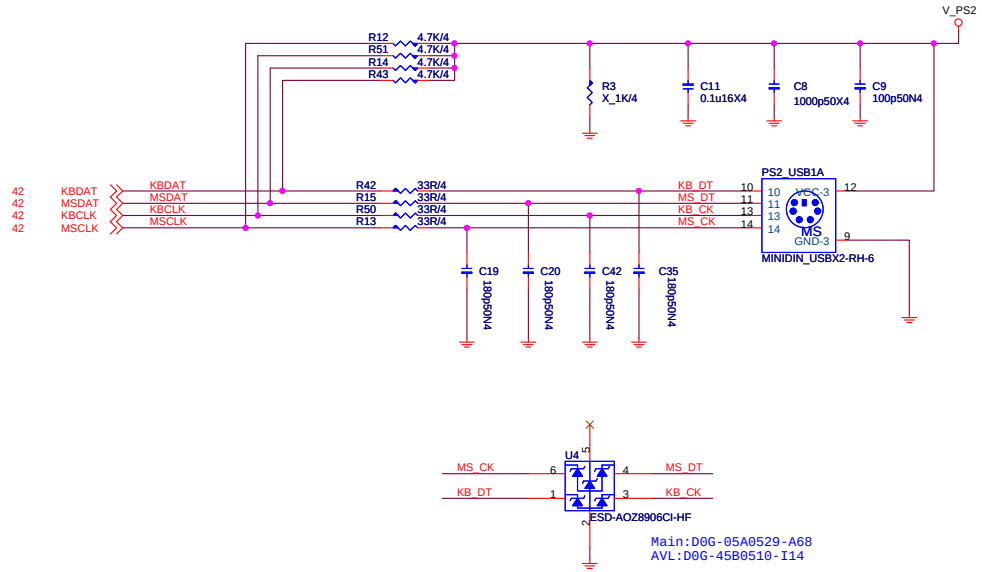
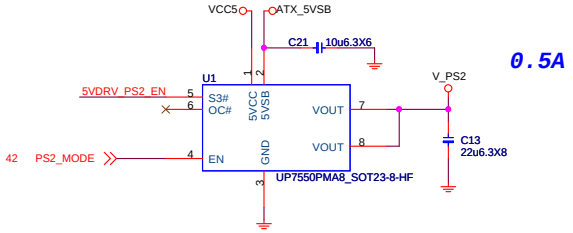
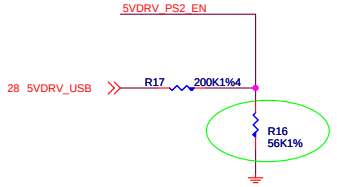
PS2 Connector



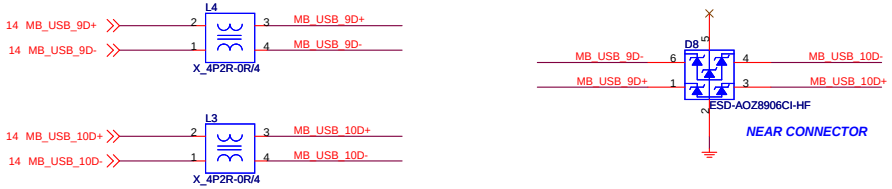
PS2 Power



USB MODE

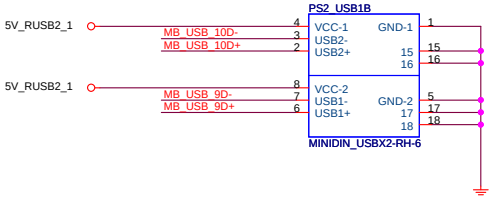


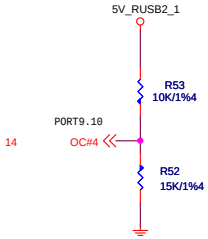
PS2 _USB



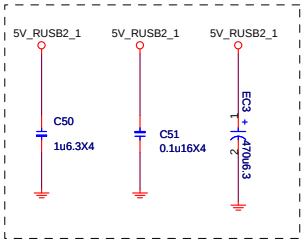
Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14

NEAR CONNECTOR



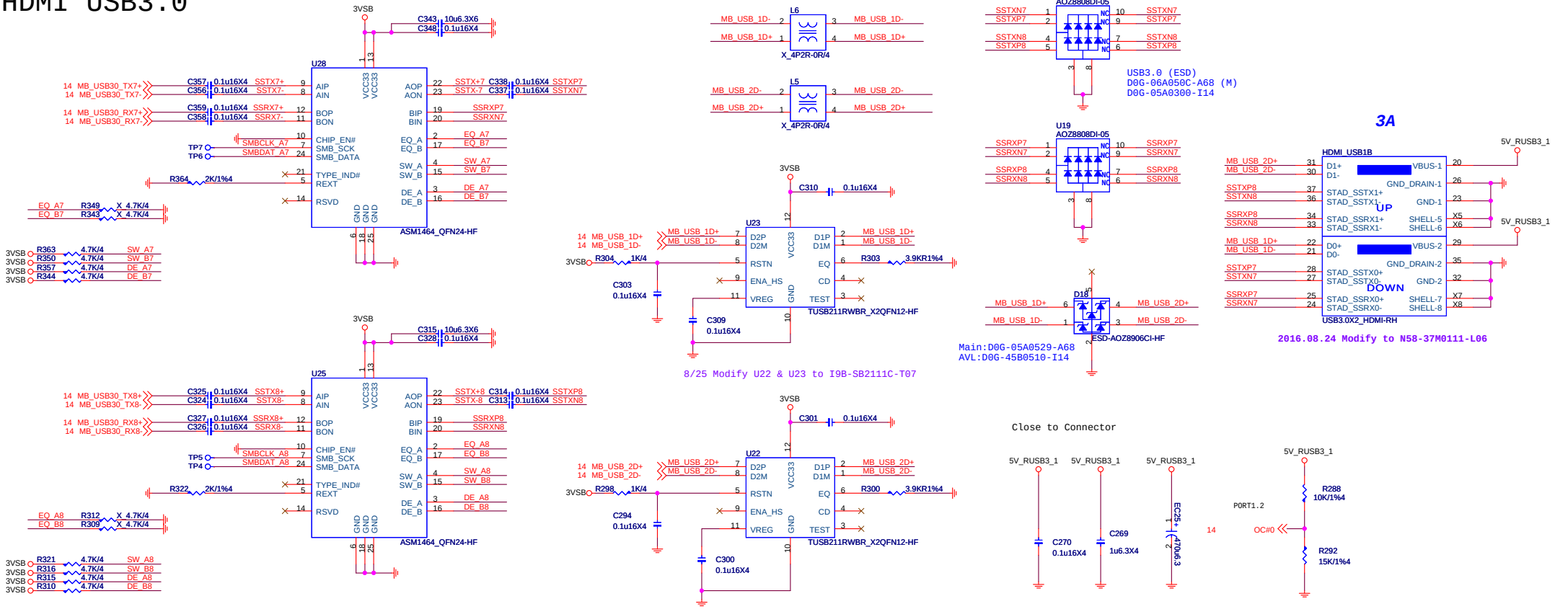


Close to Connector

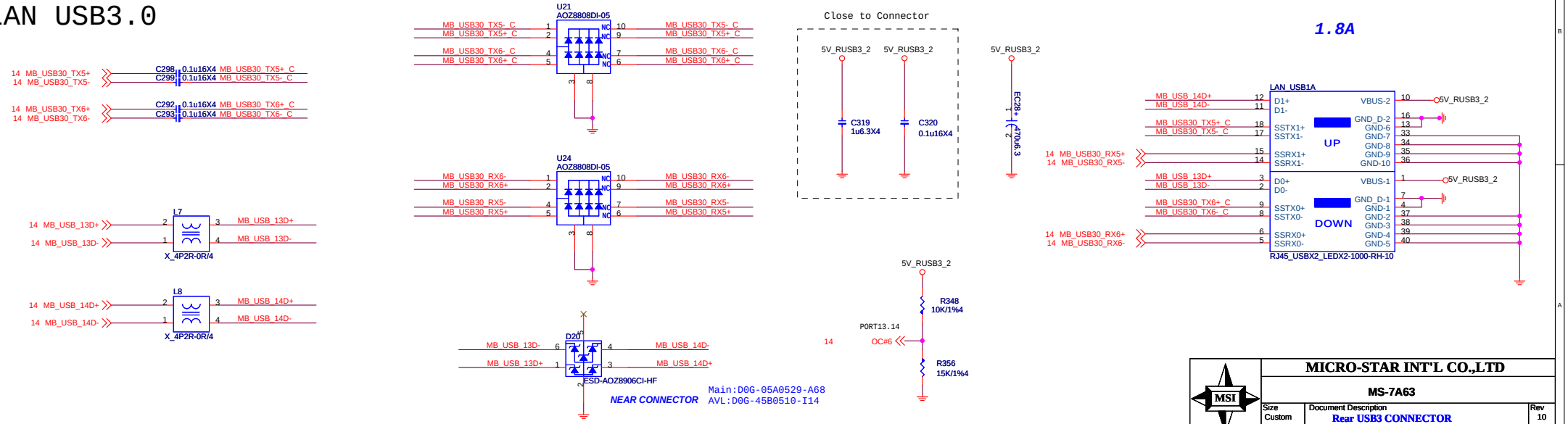


MICRO-STAR INT'L CO.,LTD		
MS-7A63		
Size: Custom	Document Description: Real USB2&PS2 CONNECTOR	Rev: 10
Date: Tuesday, September 13, 2016	Sheet 31 of 69	

HDMI USB3.0



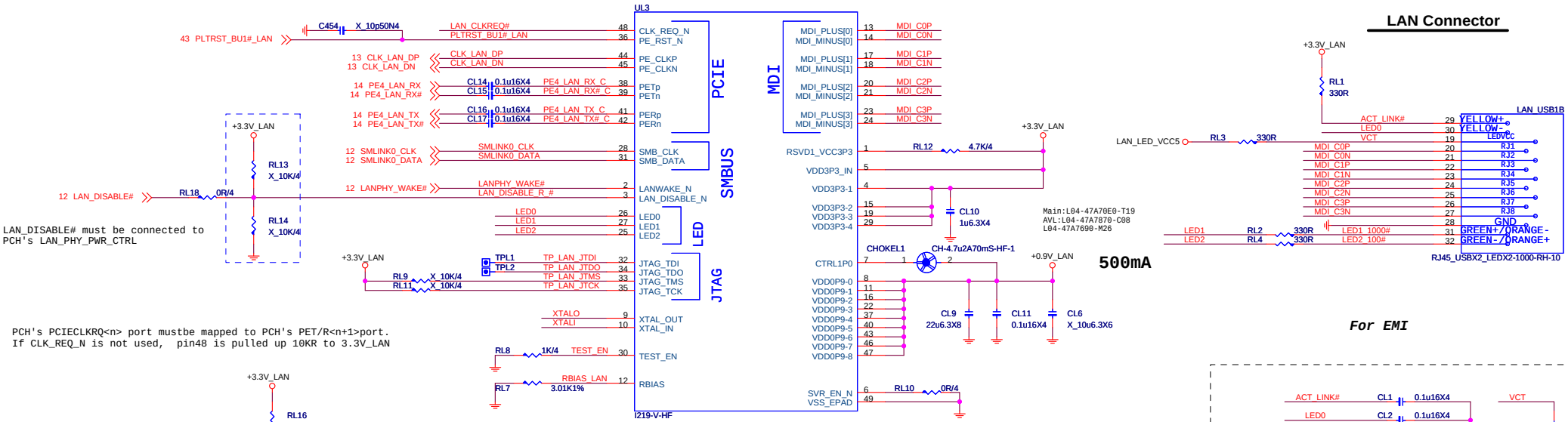
LAN USB3.0



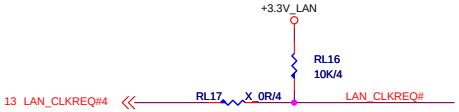
MICRO-STAR INT'L CO.,LTD	
MS-7A63	
Size: Custom	Document Description: Rear USB3 CONNECTOR
Rev: 10	
Date: Tuesday, September 13, 2016	Sheet 32 of 69

Intel Lan- i219

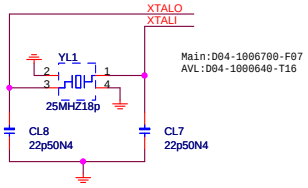
8111H:B06-08111CC-R09
8111G:B06-081116C-R09



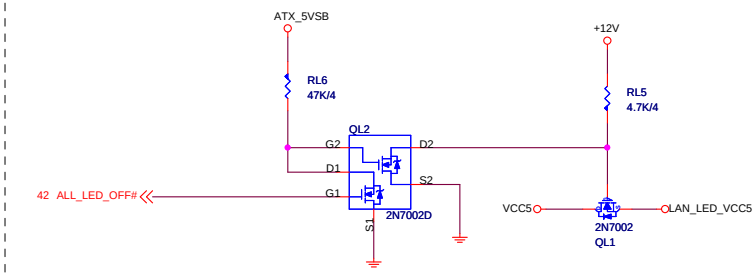
PCH's PCIECLKRQ<n> port mustbe mapped to PCH's PET/R<n+1>port.
If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN



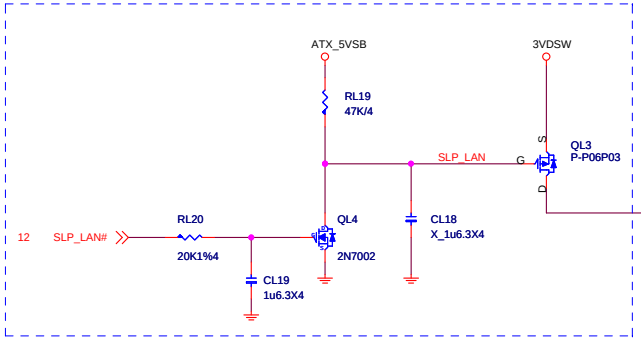
The 10Kohm pull-up resistor (RL18) of CLK_REQ_N
is connected to 3.3V Suspend/Core/etc.
power well, depending on the power well
of PCH's input PCIECLKRQ<n> buffer.

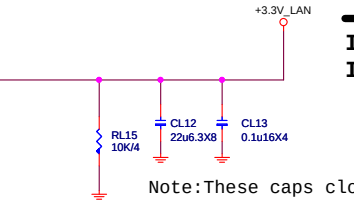


LED ON/OFF by SIO



support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



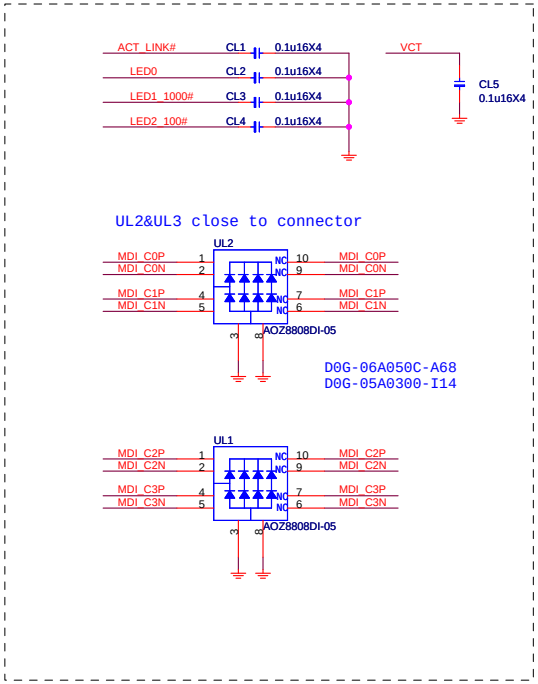


+3.3V_LAN
I218:132mA
I219:542mW

Note:These caps closed to PHY

LAN Connector

For EMI



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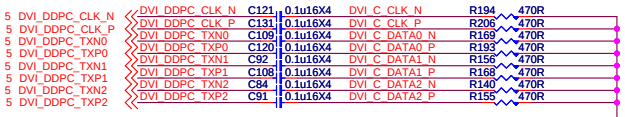
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



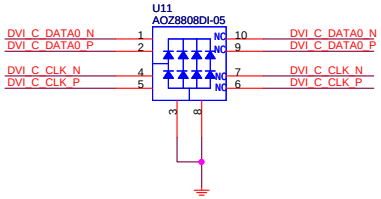
VCC3

Q29

2N7002

R207
0R/4

U26 AVL:D0G-05A050C-O05
D0G-06A050C-A68



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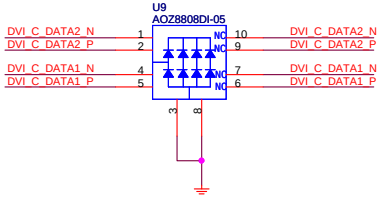
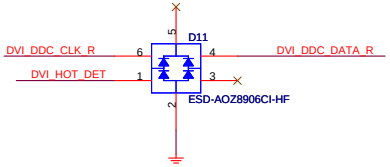
D0G-06A050C-A68





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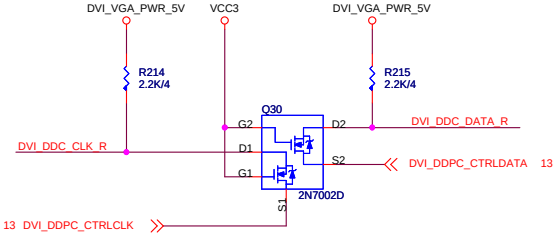

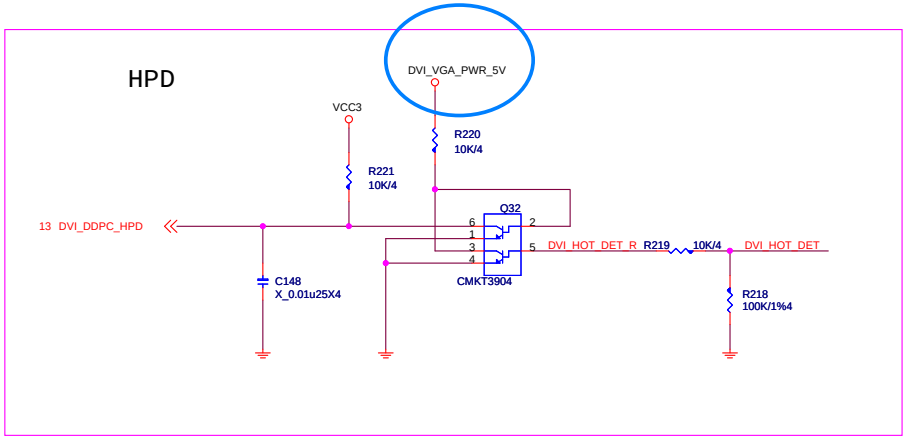

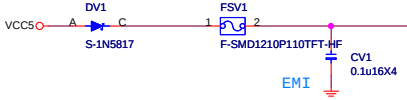

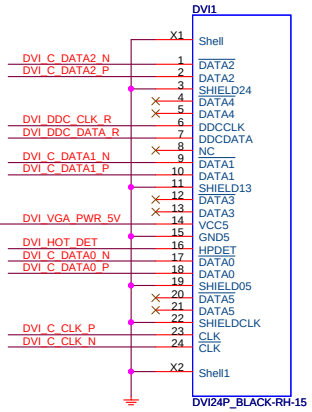

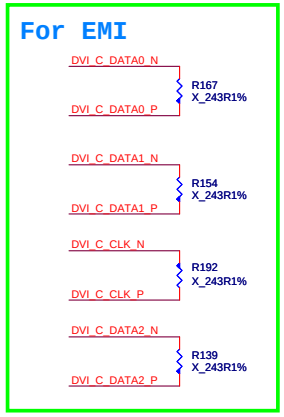

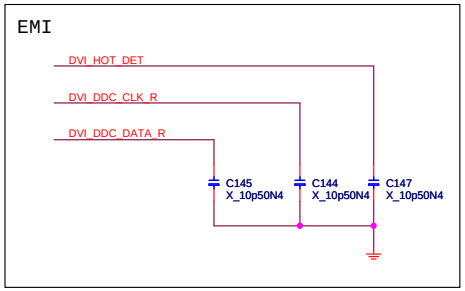

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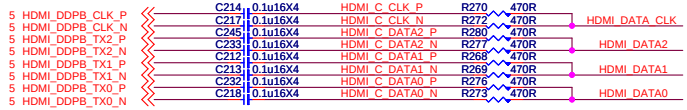
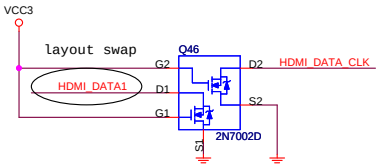
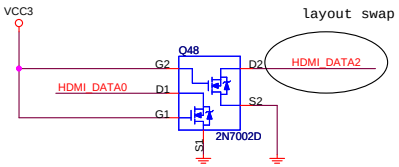
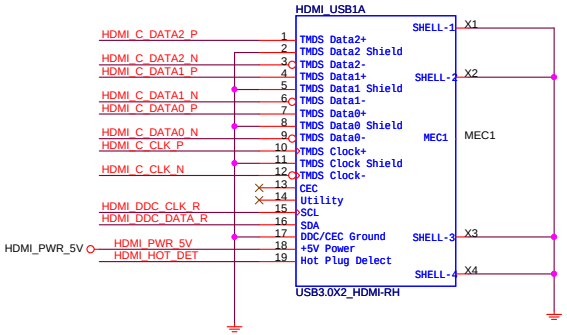
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

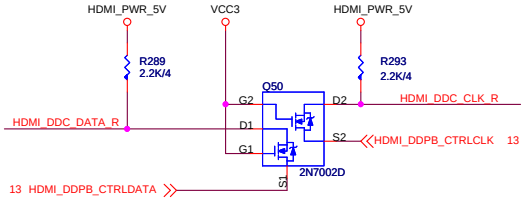


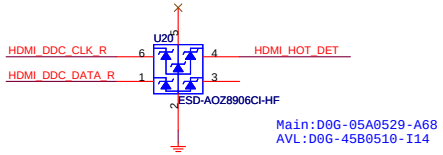






2016.08.24 Modify to N58-37M0111-L06





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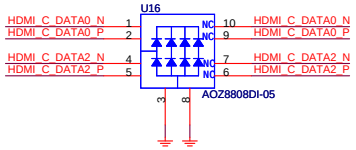
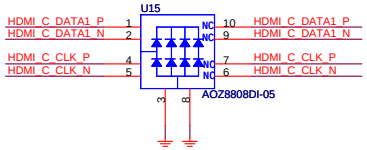
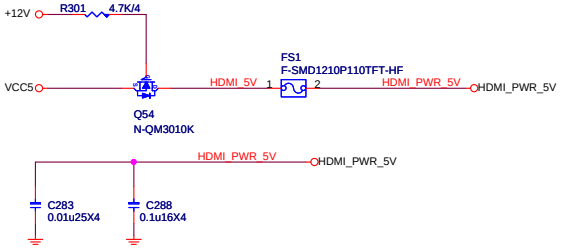
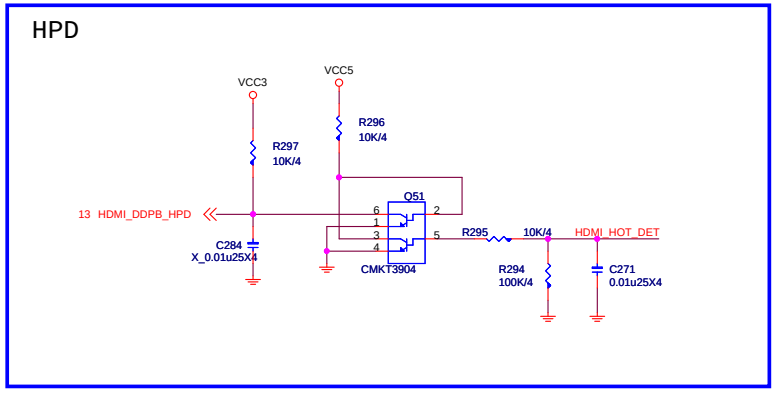
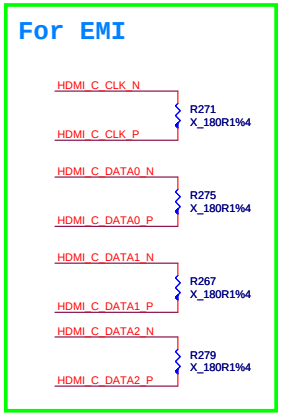
AVL:D0G-45B0510-I14











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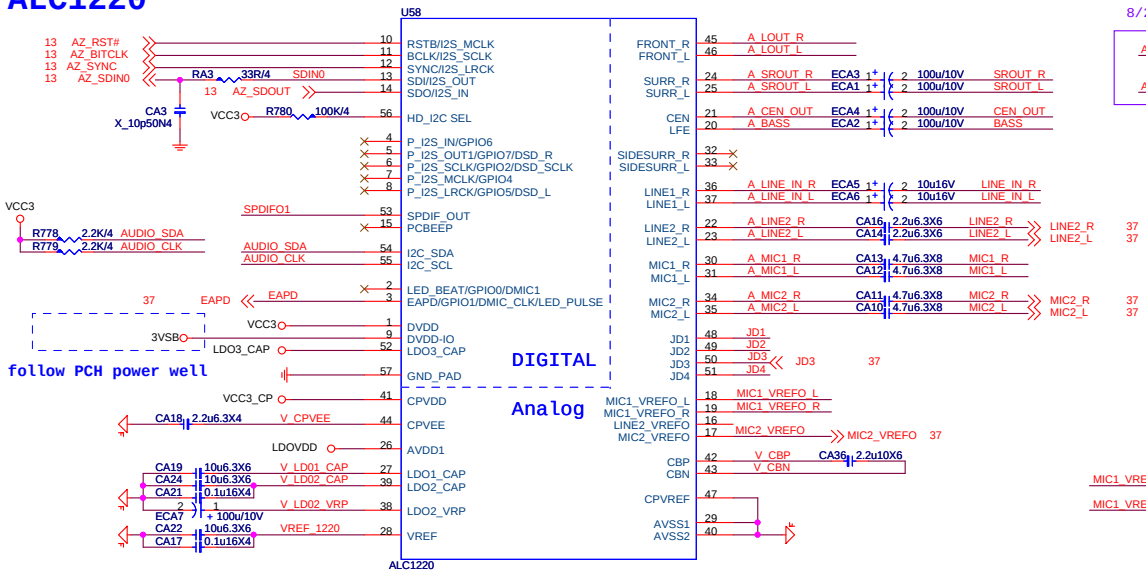
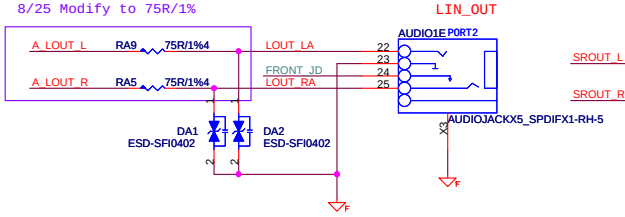
ALC1220

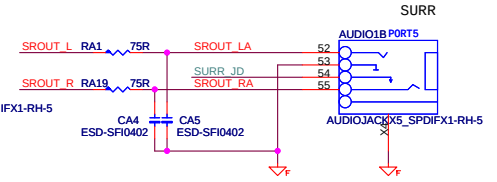


8/25 Modify to 75R/1%

LIN_OUT

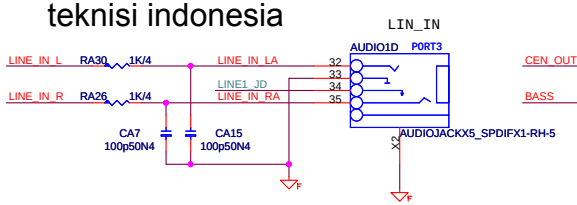


SURR

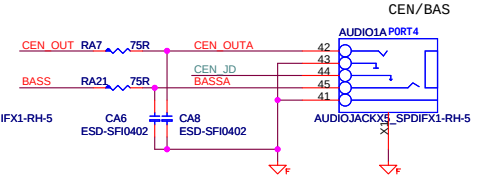


teknisi indonesia

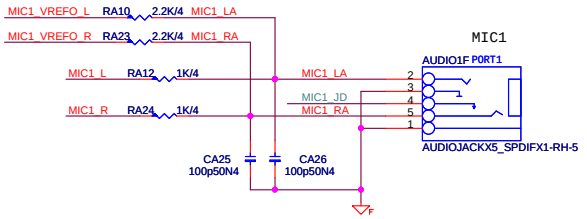
LIN_IN



CEN/BAS



MIC1



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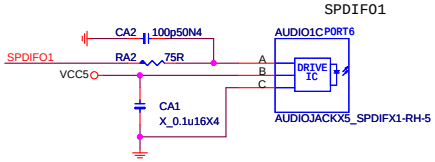
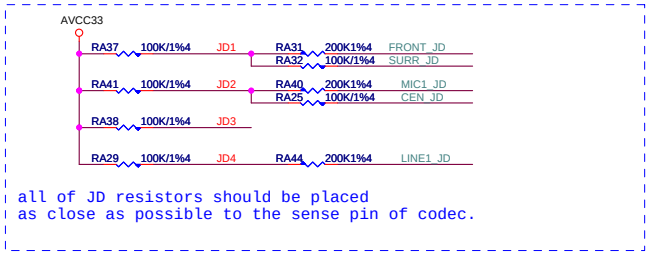
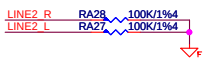
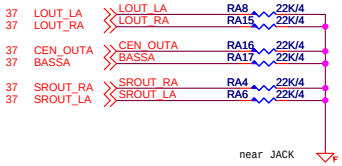
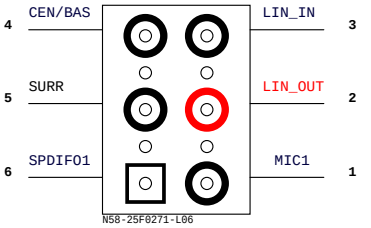


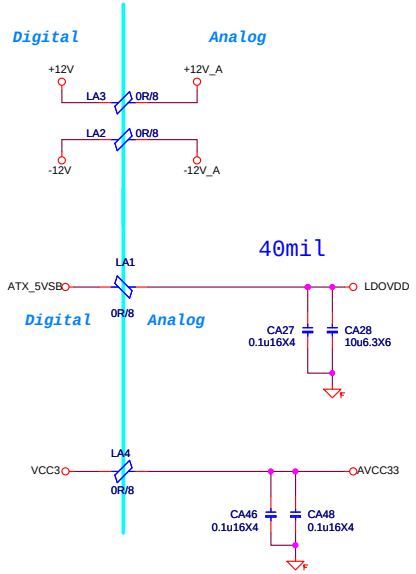


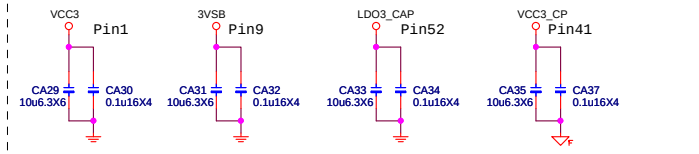


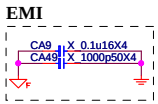


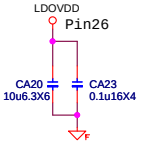
For GAMING





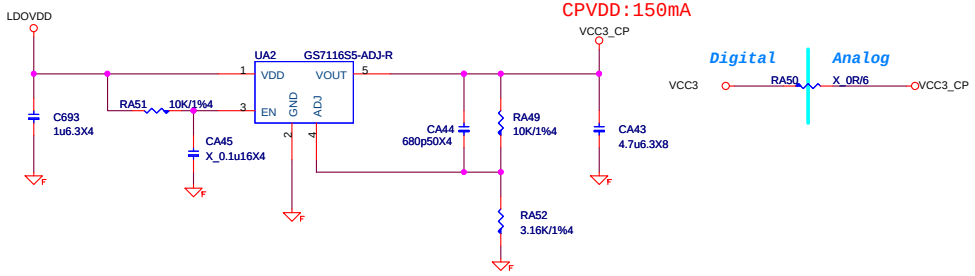






CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V

CPVDD:150mA



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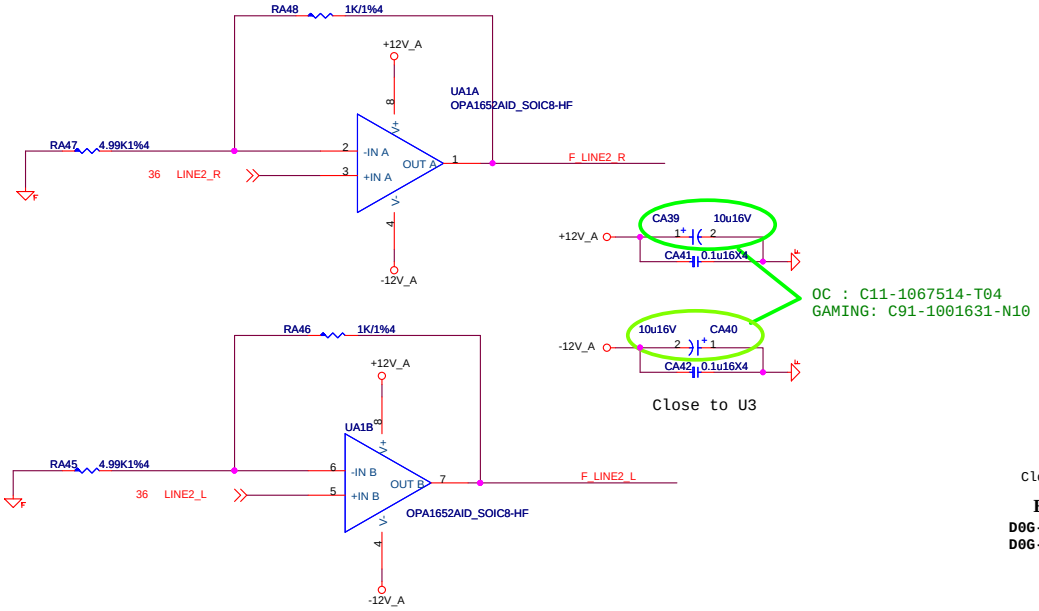
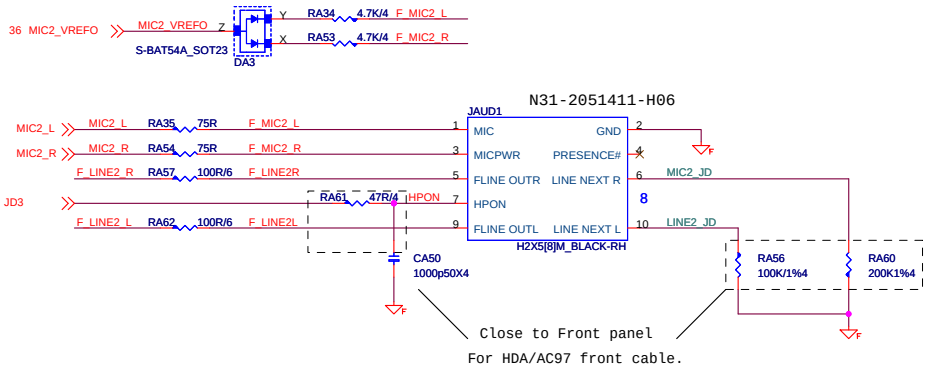


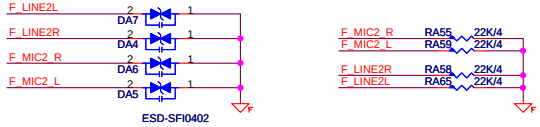


Close to Jack

ESD protect

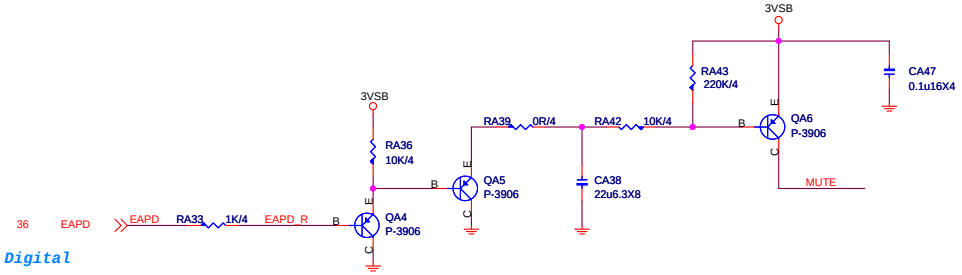
D0G-2710510-I05

D0G-2950500-SI0



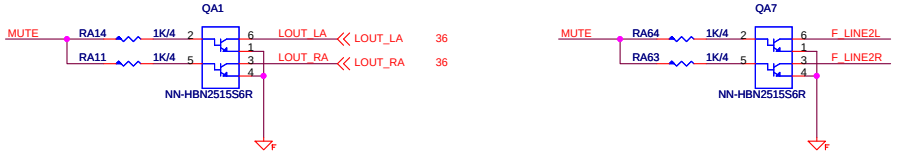
Rear Line OUT De-POP circuit

(De-pop circuit for Rear Line out & Front Headphone out)

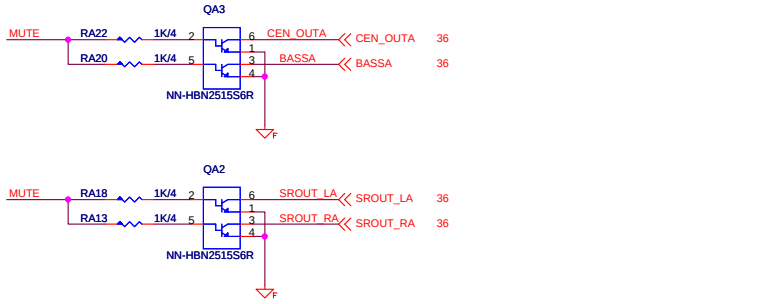


Digital

Analog



(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA4,CA5, CA6, CA8,to TVS)



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MS-7A63		
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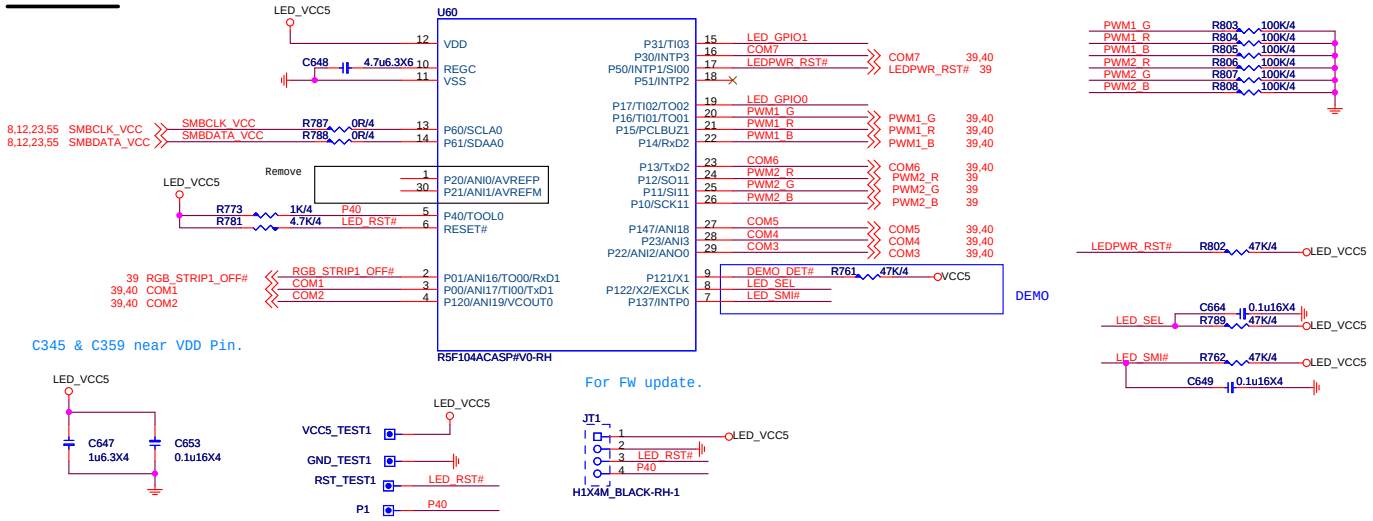
LED MCU



Control	Net Name	PWM USE	Connector
PCH	LED_GPIO1	No Use	JPIPE_LED2
Audio	COM1~7	PWM1	RGB LED
Board Side LED	COM1~7	PWM2	RGB LED
LED STRIPLINE	RGB_STRIP1_OFF#	PWM1	JLED1
IO Cover	LED_GPIO0	No Use	JPIPE_LED1

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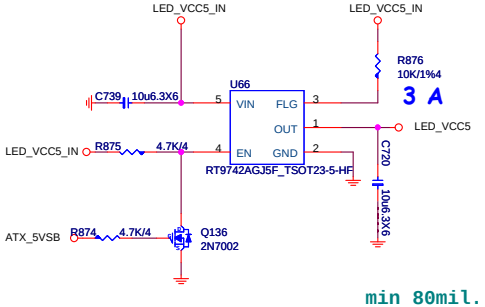
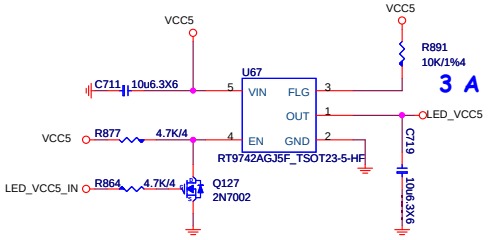
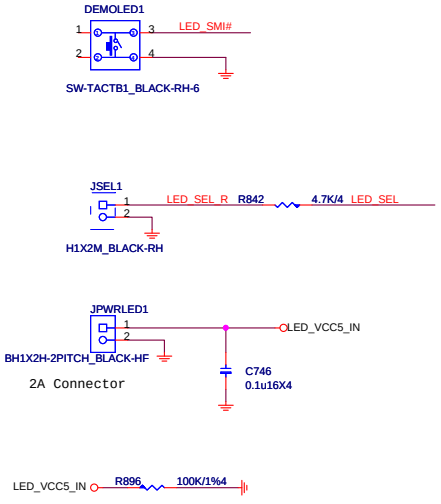
EXTERNAL POWER INPUT



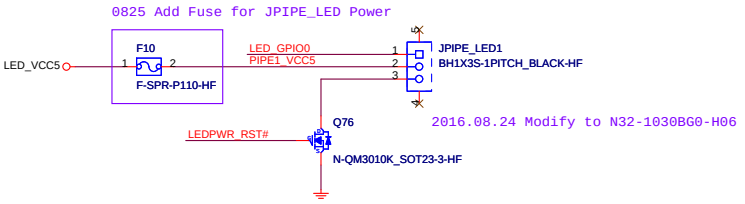


LED Demo Button



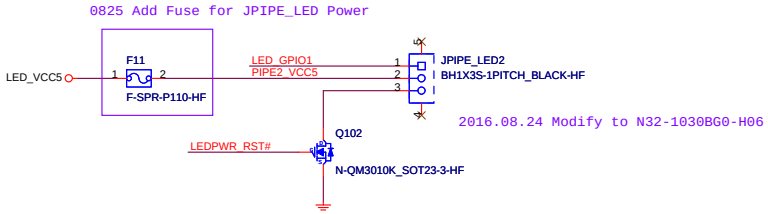
Cover LED

6PCS LED*0.16W=0.96W



HEATSINK LED

9PCS LED*0.16W=1.44W



MICRO-STAR INT'L CO.,LTD

MS-7A63

Size	Document Description	Rev
Custom	LED MCU Control	10

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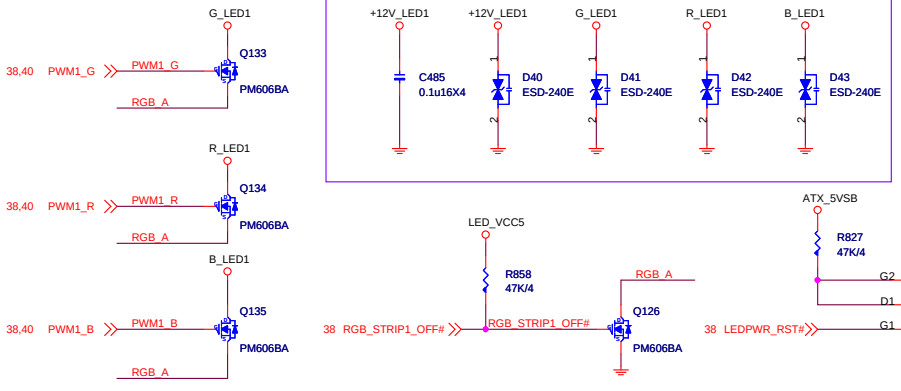
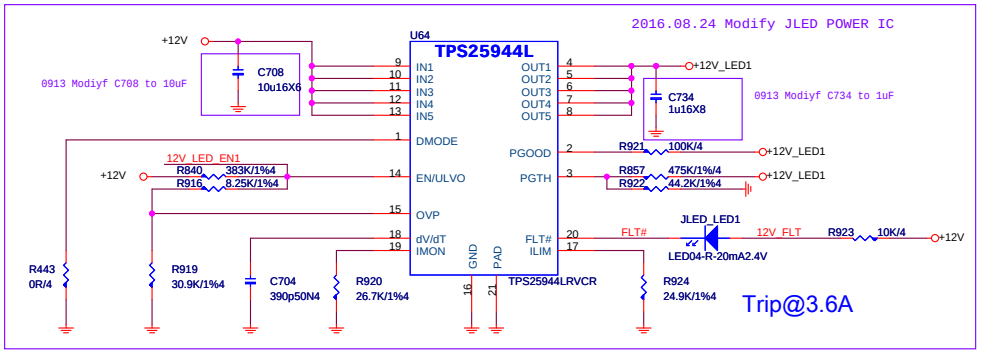
LED STRIPLINE(LEFT)

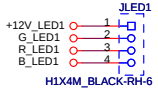
2016.08.24 Add,Close to JLED1

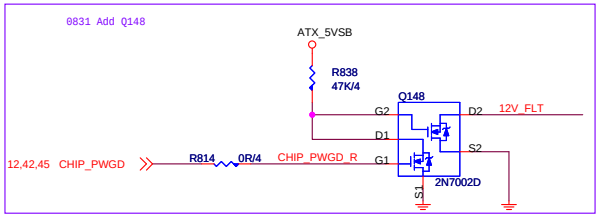


外接LED 燈條 (RGB)
---- PCB 文字面 (JLED1)
---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺 (待7A20驗證)

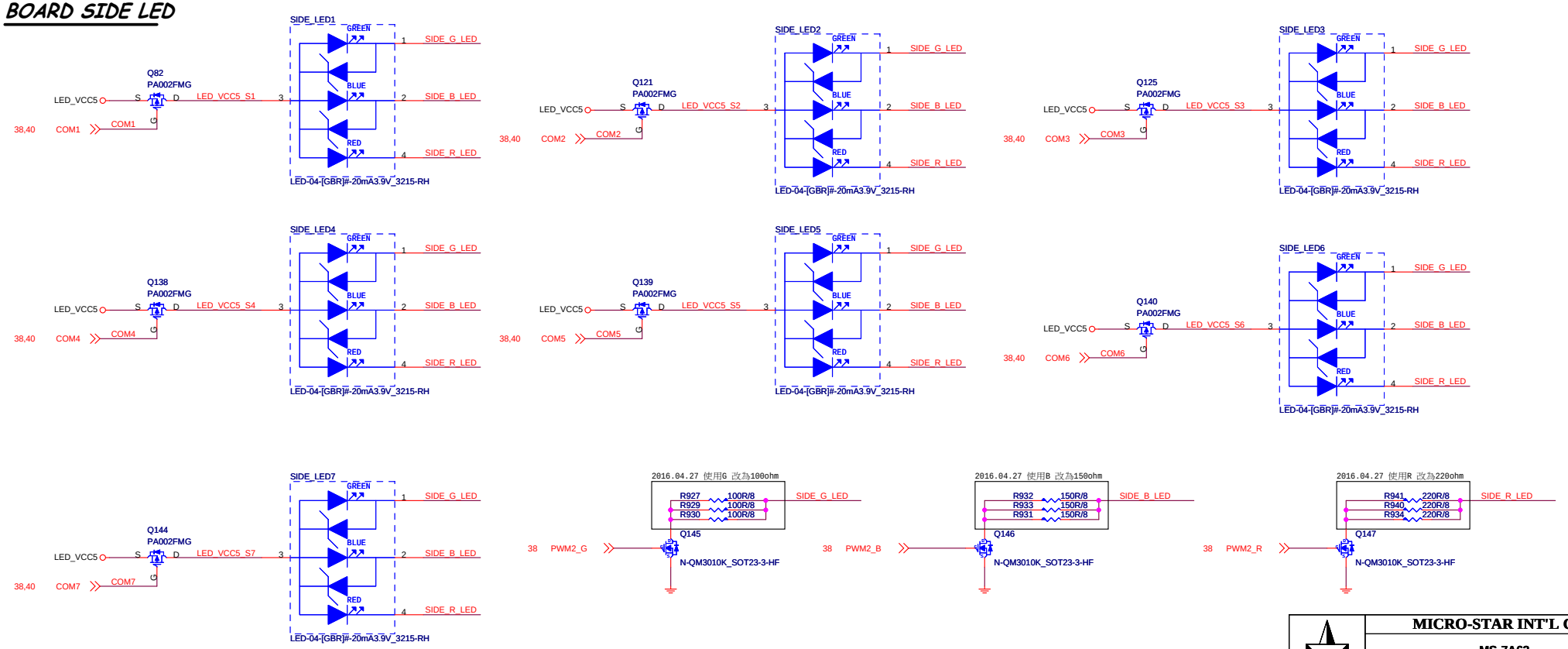
2016.08.24 Modify JLED POWER IC







BOARD SIDE LED



MICRO-STAR INT'L CO.,LTD		
MS-7A63		
Size: Custom	Document Description: LED STRIPLINE/BOARD SIDE LED	Rev: 10
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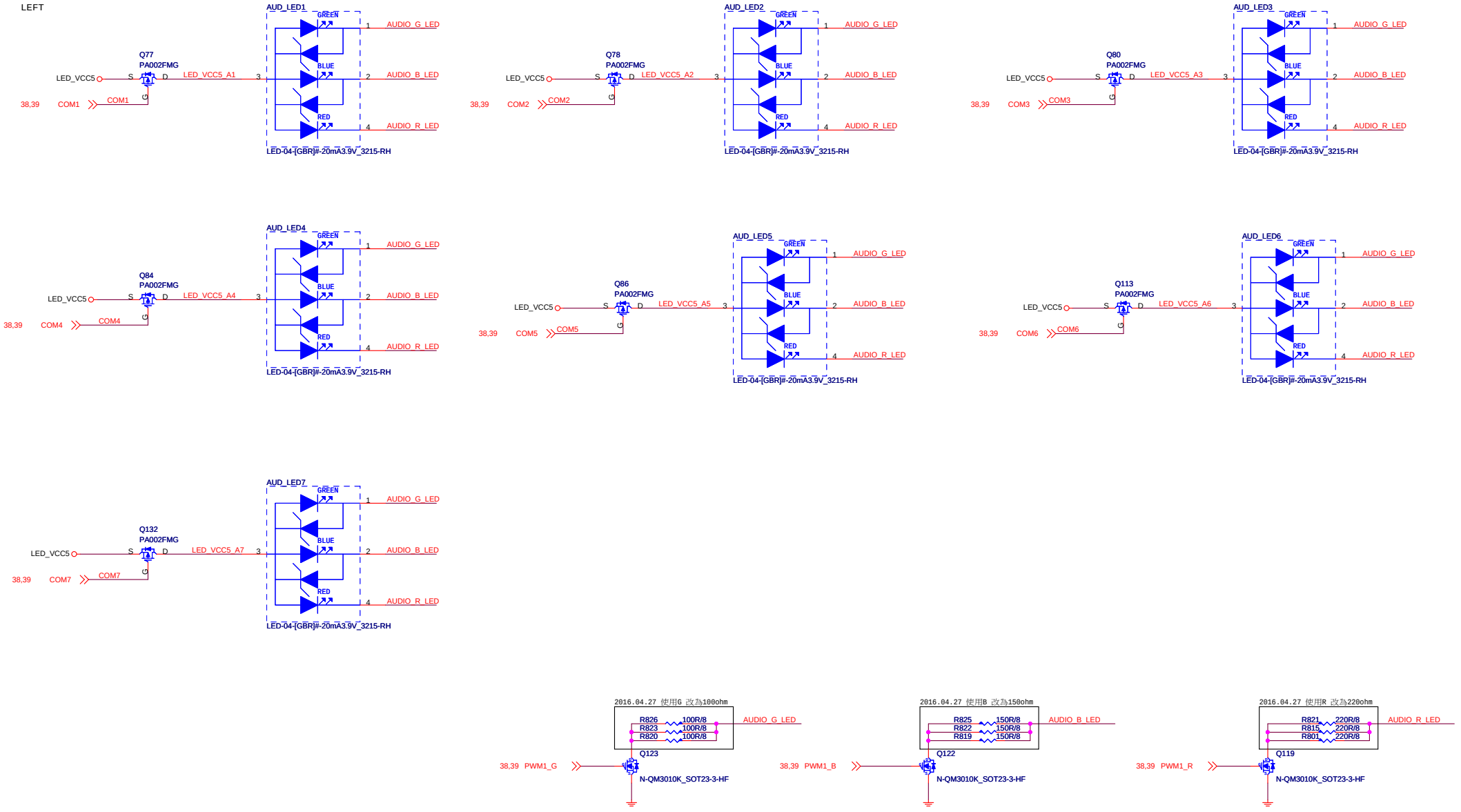
AUDIO_MOAT LED

LEFT



MSI	MICRO-STAR INT'L CO.,LTD	
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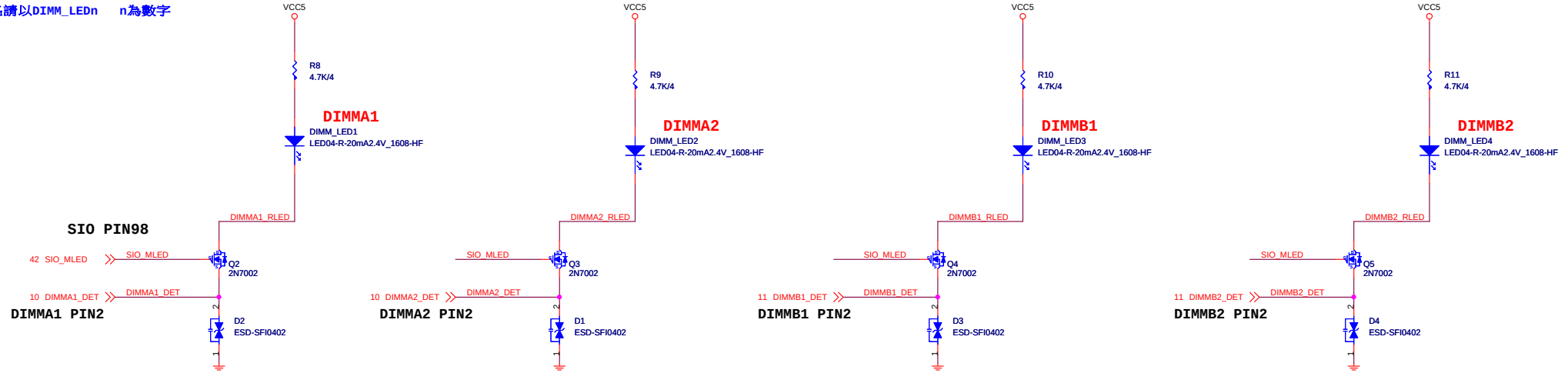
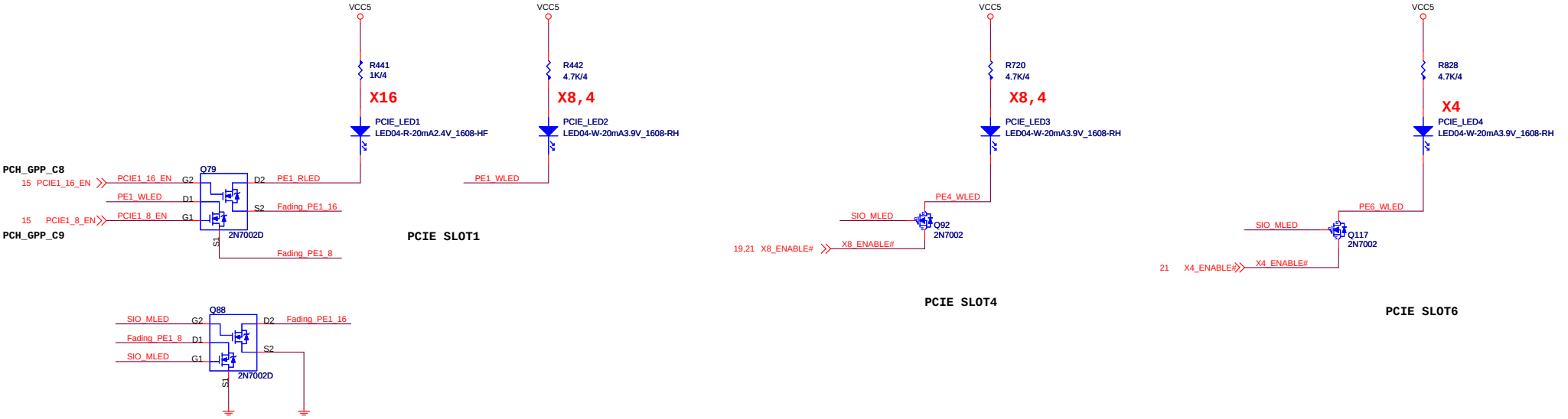
DIMM_SLOT

紅 : D0C-040S500-E07

LED 命名請以DIMM_LEDn n為數字



PCIE SLOT LED



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A63	
Size: Custom	Document Description: LED DIMM/PCIE	Rev: 10
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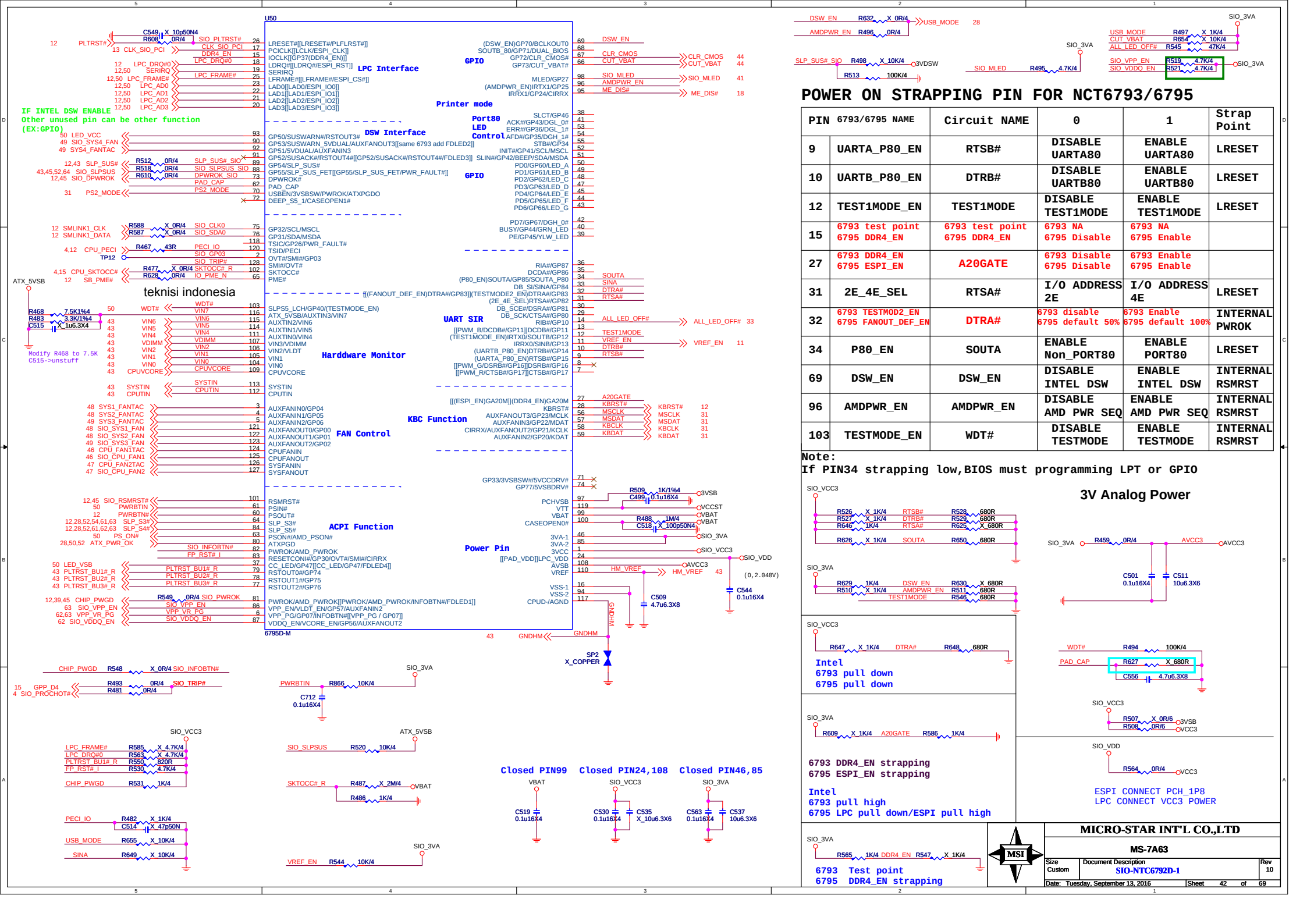
U50
LPC Interface
DSW Interface
GPIO
Printer mode
Port80
LED
Control
GPIO
UART SIR
Harddware Monitor
KBC Function
FAN Control
ACPI Function
Power Pin
IF INTEL DSW ENABLE
Other unused pin can be other function
(EX:GPIO)
teknisi indonesia
Modify R468 to 7.5K
C515->unstuff
6795D-M
POWER ON STRAPPING PIN FOR NCT6793/6795
PIN
6793/6795 NAME
Circuit NAME
0
1
Strap Point
9
UARTA_P80_EN
RTSB#
DISABLE UARTA80
ENABLE UARTA80
LRESET
10
UARTB_P80_EN
DTRB#
DISABLE UARTB80
ENABLE UARTB80
LRESET
12
TEST1MODE_EN
TEST1MODE
DISABLE TEST1MODE
ENABLE TEST1MODE
LRESET
15
6793 test point
6795 DDR4_EN
6793 test point
6795 DDR4_EN
6793 NA
6795 Disable
6793 NA
6795 Enable
27
6793 DDR4_EN
6795 ESPI_EN
A20GATE
6793 Disable
6795 Disable
6793 Enable
6795 Enable
31
2E_4E_SEL
RTSA#
I/O ADDRESS 2E
I/O ADDRESS 4E
LRESET
32
6793 TESTMOD2_EN
6795 FANOUT_DEF_EN
DTRA#
6793 disable
6795 default 50%
6793 Enable
6795 default 100%
INTERNAL PWROK
34
P80_EN
SOUTA
ENABLE Non_PORT80
ENABLE PORT80
LRESET
69
DSW_EN
DSW_EN
DISABLE INTEL DSW
ENABLE INTEL DSW
INTERNAL RSMRST
96
AMDPWR_EN
AMDPWR_EN
DISABLE AMD PWR SEQ
ENABLE AMD PWR SEQ
INTERNAL RSMRST
103
TESTMODE_EN
WDT#
DISABLE TESTMODE
ENABLE TESTMODE
INTERNAL RSMRST
Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO
3V Analog Power
Intel
6793 pull down
6795 pull down
6793 DDR4_EN strapping
6795 ESPI_EN strapping
Intel
6793 pull high
6795 LPC pull down/ESPI pull high
6793 Test point
6795 DDR4_EN strapping
ESPI CONNECT PCH_1P8
LPC CONNECT VCC3 POWER
Closed PIN99
Closed PIN24,108
Closed PIN46,85
MICRO-STAR INT'L CO.,LTD
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Size
Custom
Document Description
SIO-NTC6792D-1
Rev
10
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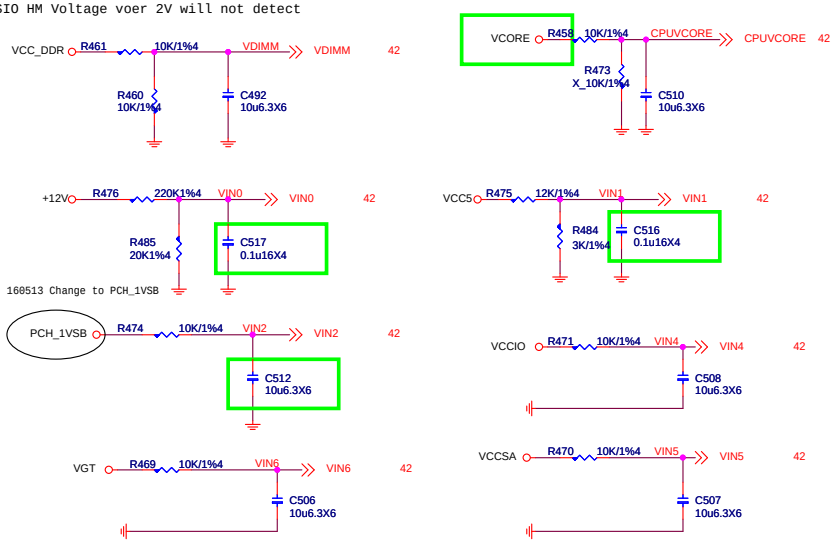
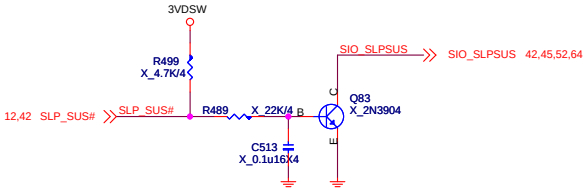
HW Monitor - Voltage

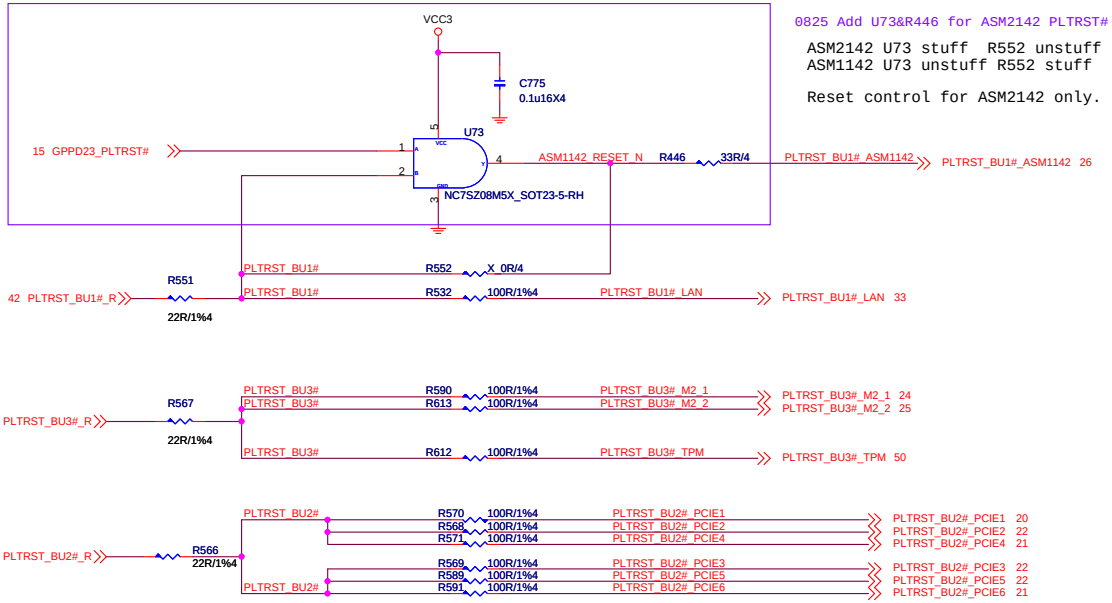
SIO HM Voltage voer 2V will not detect



SLP_SUS Co-lay circuit



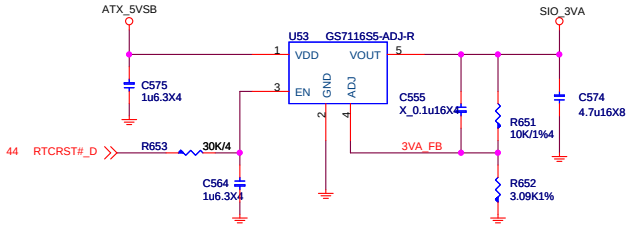
Thermal Monitor



0825 Add U73&R446 for ASM2142 PLTRST#

ASM2142 U73 stuff R552 unstuff
ASM1142 U73 unstuff R552 stuff

Reset control for ASM2142 only.



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	SIO-NTC6792D-2	10

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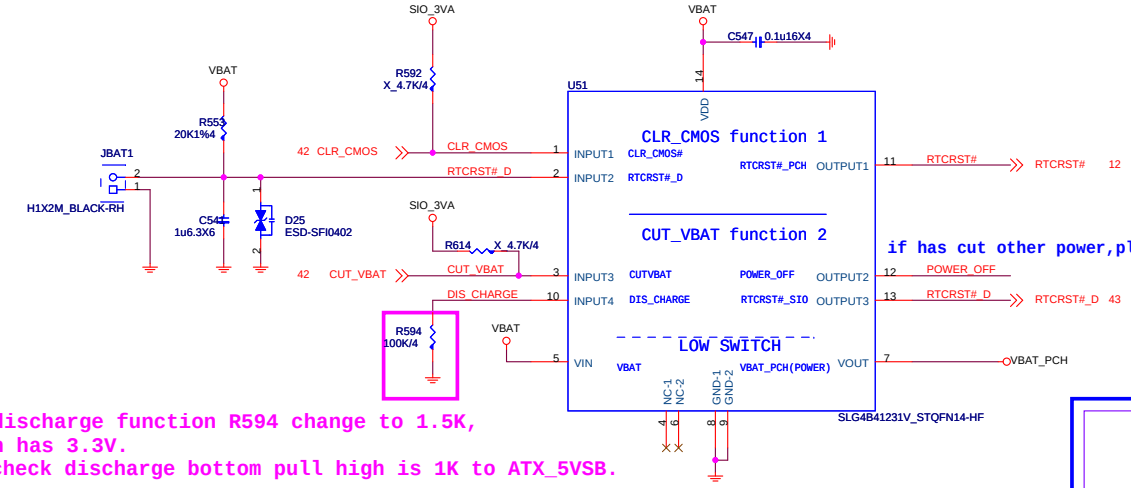
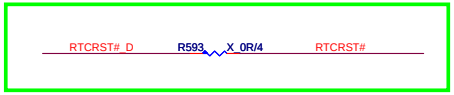
CLR_CMOS



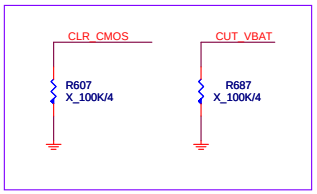
if has cut other power,please use output 2.

If has discharge function R594 change to 1.5K,
this pin has 3.3V.
please check discharge bottom pull high is 1K to ATX_5VSB.



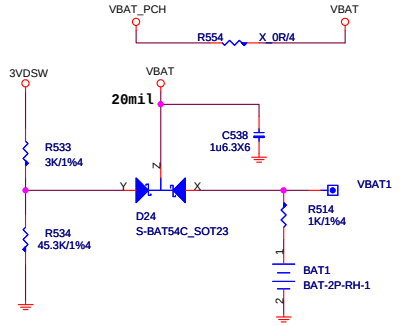
Co-Lay NOT USE U12 , R139 STUFF

If STUFF R139 Please Check RTCRST# Double Pull High

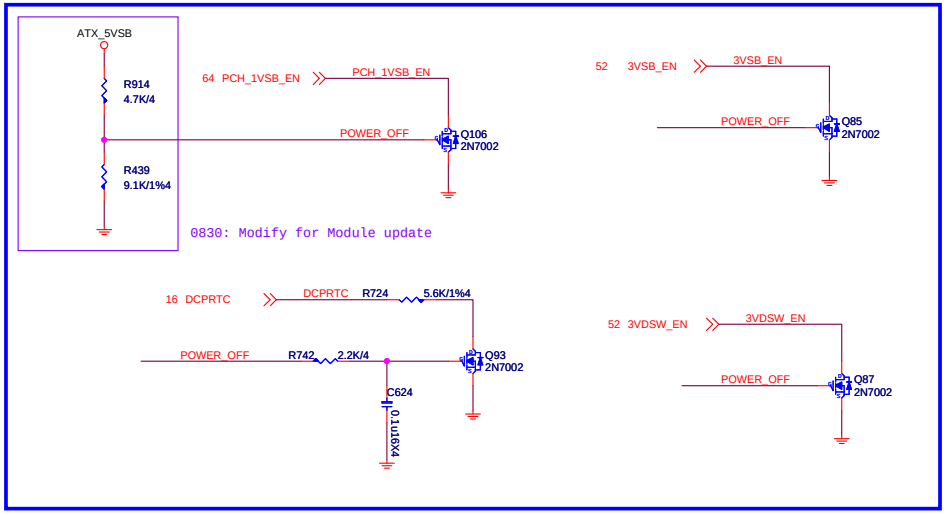


0830: Add R607.R687 for Module update

VBAT



Co-Lay NOT USE U12 , ALL UNSTUFF



Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

Function 2				
IN		OUT		
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

Default

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	Clear CMOS/CUT VBAT	10

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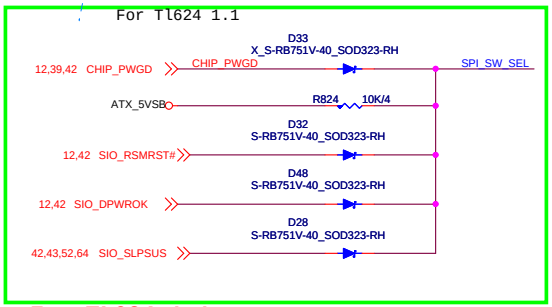
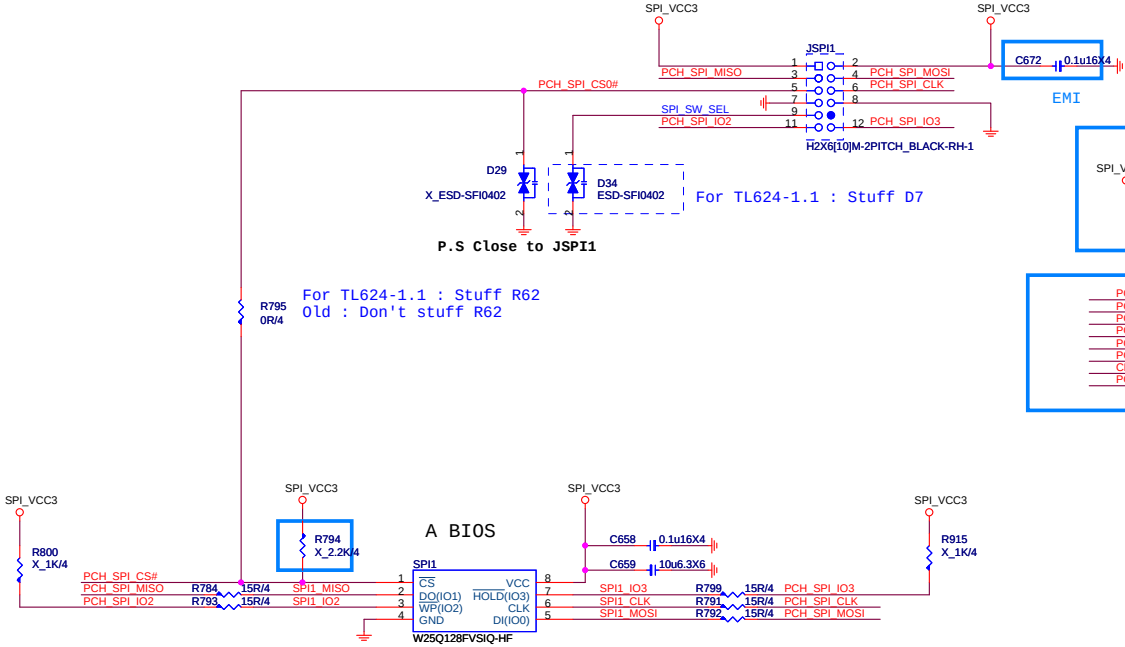
Module Stuff CHIP_PWGD,
But PCH_PWROK may ramp up before CHIP_PWGD.

0825 Add D48,unstuff D33

For Tl624 1.1



For TL624-1.1
SKYLAKE : Stuff D10/D17/R353
B85/H87 : Stuff D8/D9/R353
Others : Stuff R272



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MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A63	
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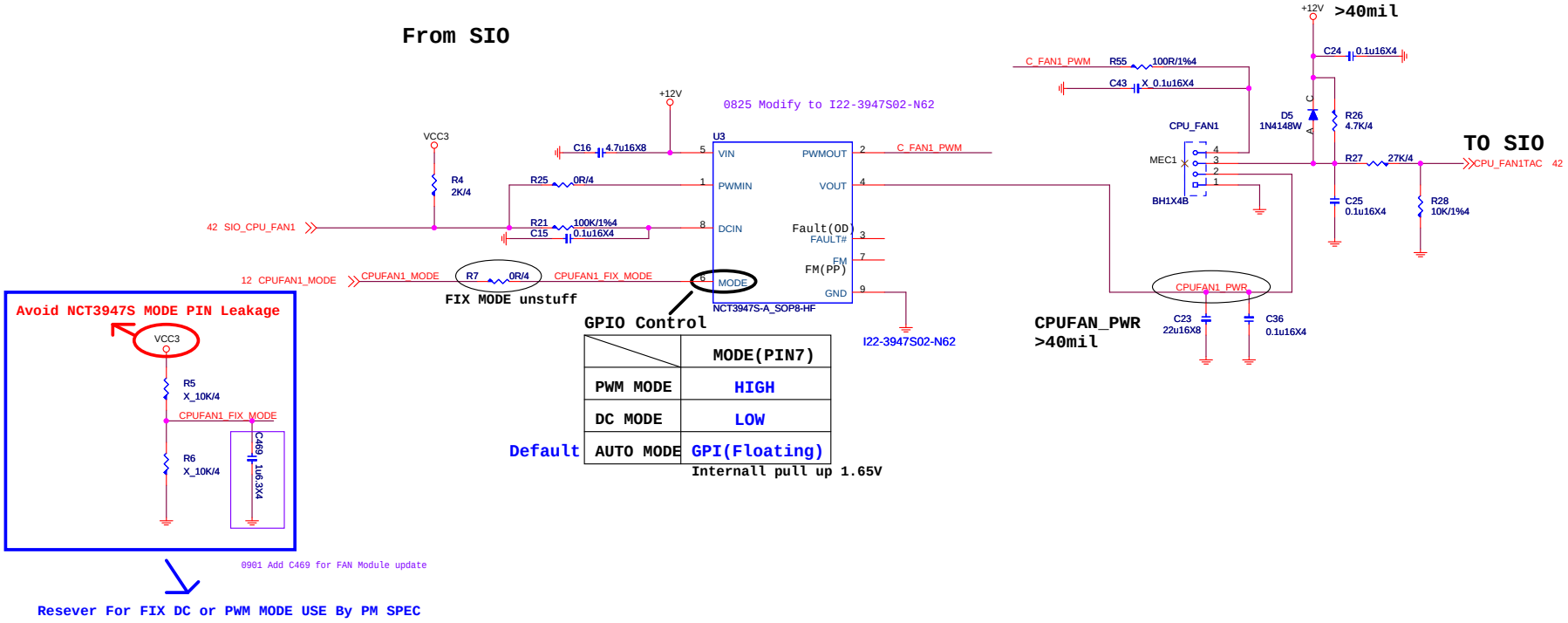

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

1.MODE : USE MODE PIN change FAN MODE(PWM or DC FAN)
2.FAULT : USE FAULT PIN Triger OVT/OCP Protection,LOW Atcive (Reserve NEW IC)
3.FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	CPU FAN1	10

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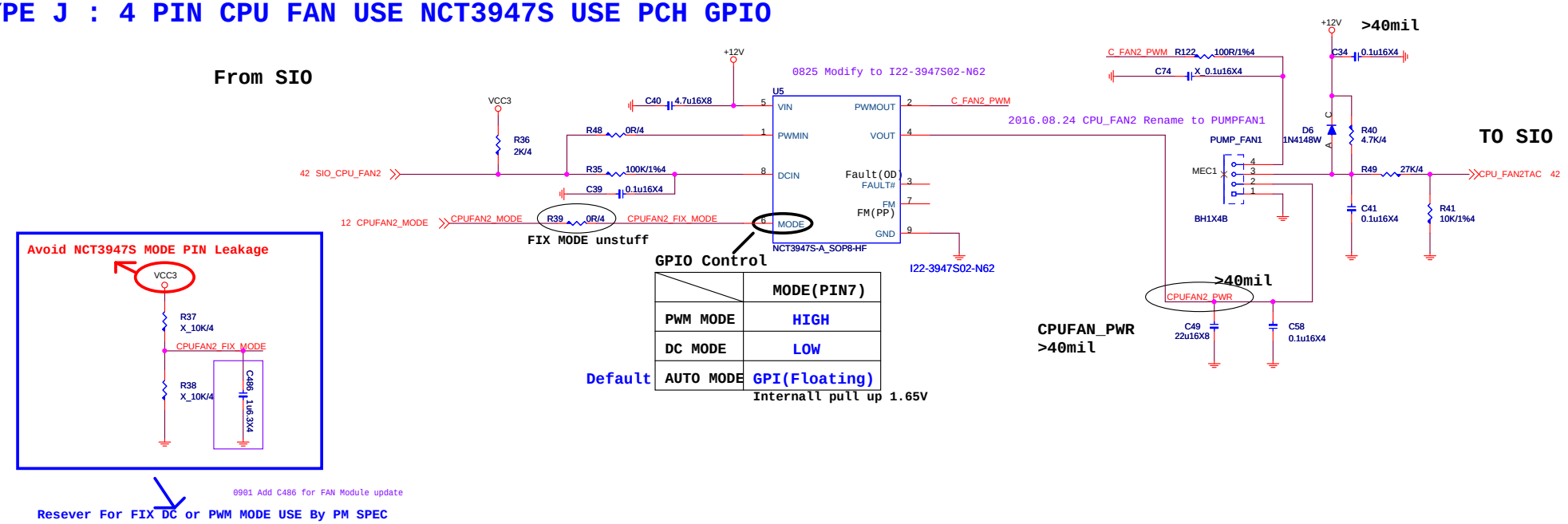
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

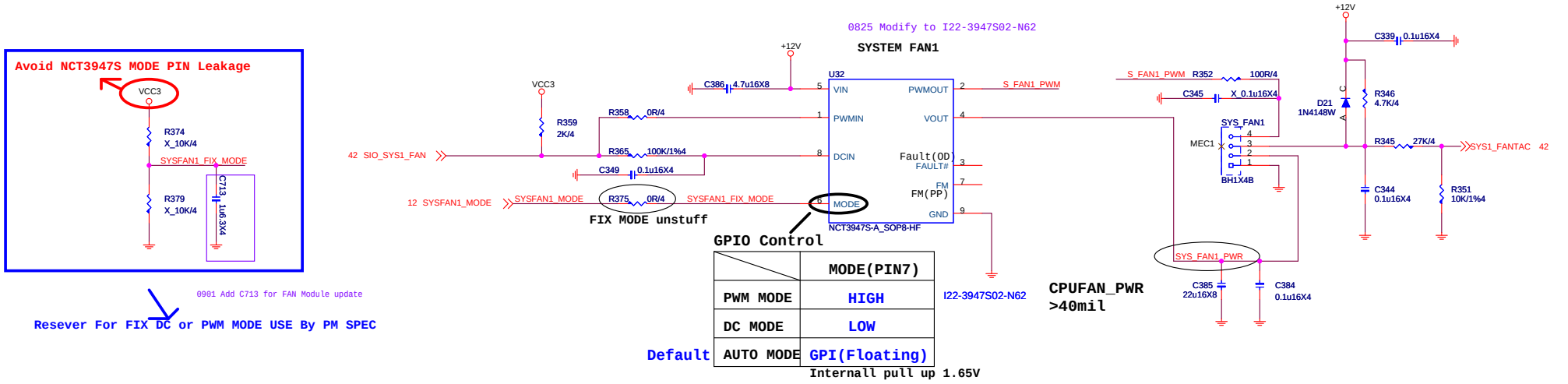
0901 Add C486 for FAN Module update

Resever For FIX DC or PWM MODE USE By PM SPEC

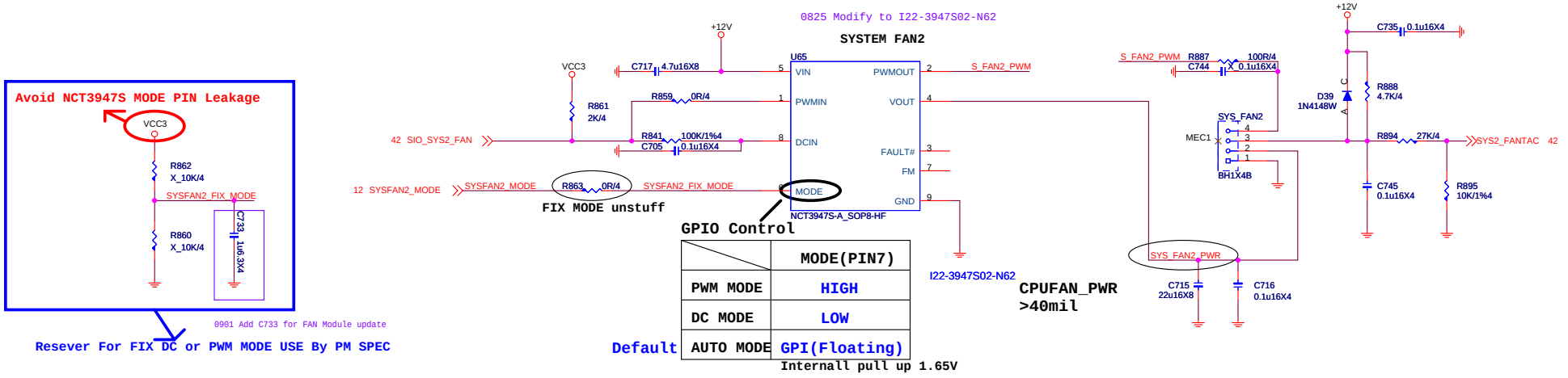
1.MODE : USE MODE PIN change FAN MODE(PWM or DC FAN)
2.FAULT : USE FAULT PIN Triger OVT/OCP Protection,LOW Atcive (Reserve NEW IC)
3.FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)

MICRO-STAR INT'L CO.,LTD		
MS-7A63		
Size: Custom	Document Description: PUMPFAN1	Rev: 10
Date: Tuesday, September 13, 2016	Sheet 47 of 69	

TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	SYSTEM FAN1&2	10

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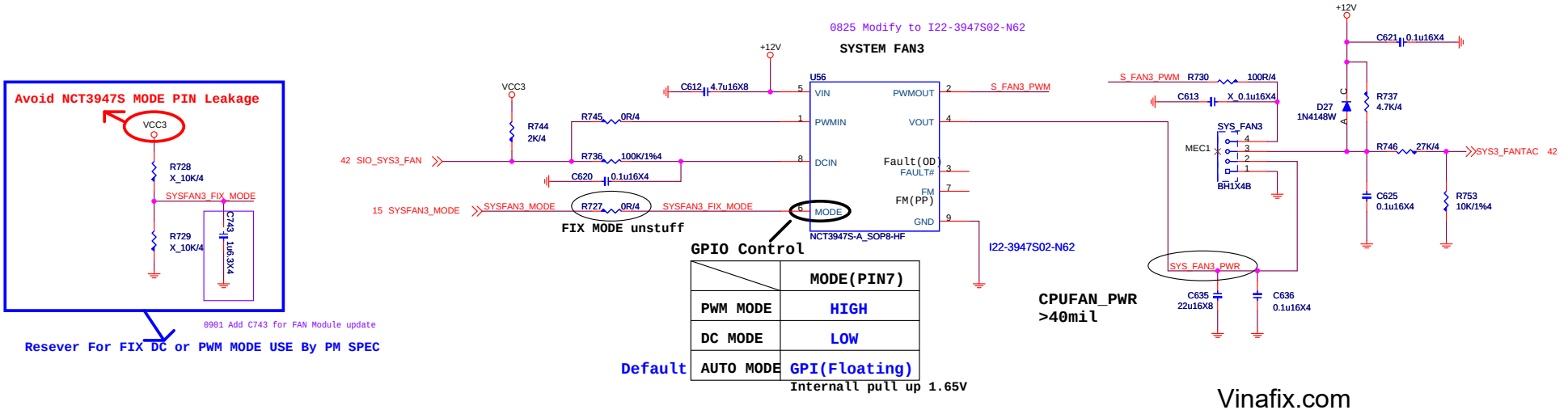
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

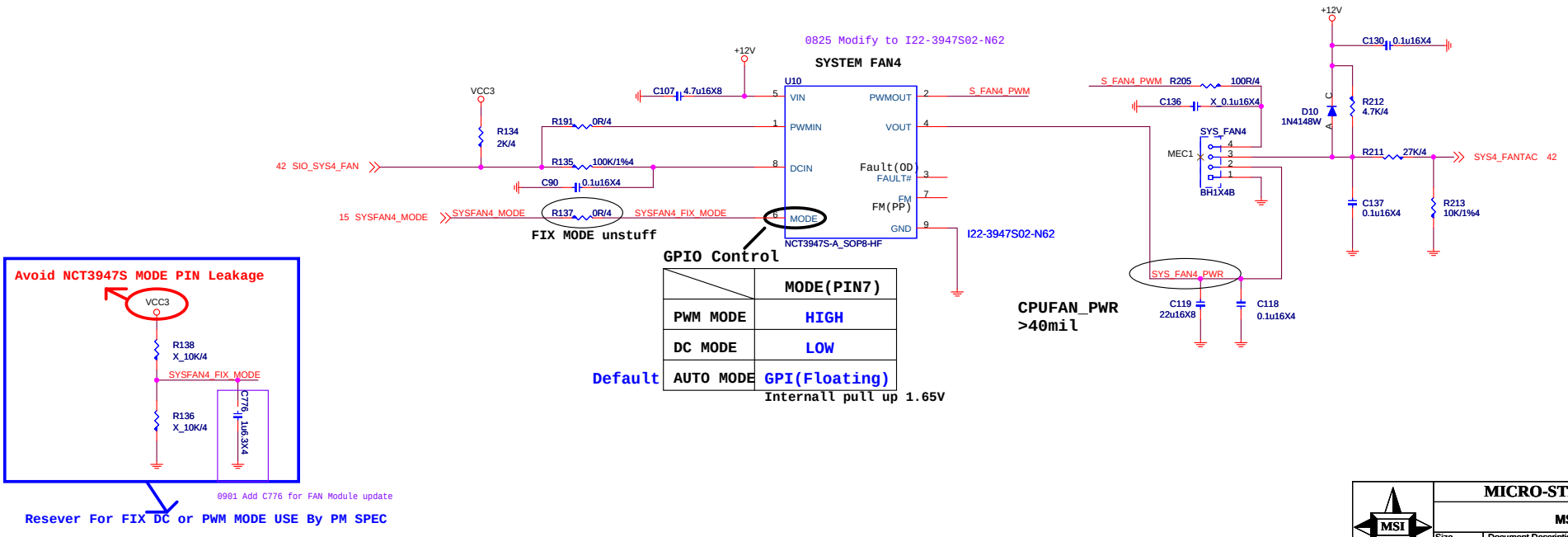


	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

Vinafix.com

TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

MICRO-STAR INT'L CO.,LTD		
MS-7A63		
Size: Custom	Document Description: SYSTEM FAN3&4	Rev: 10
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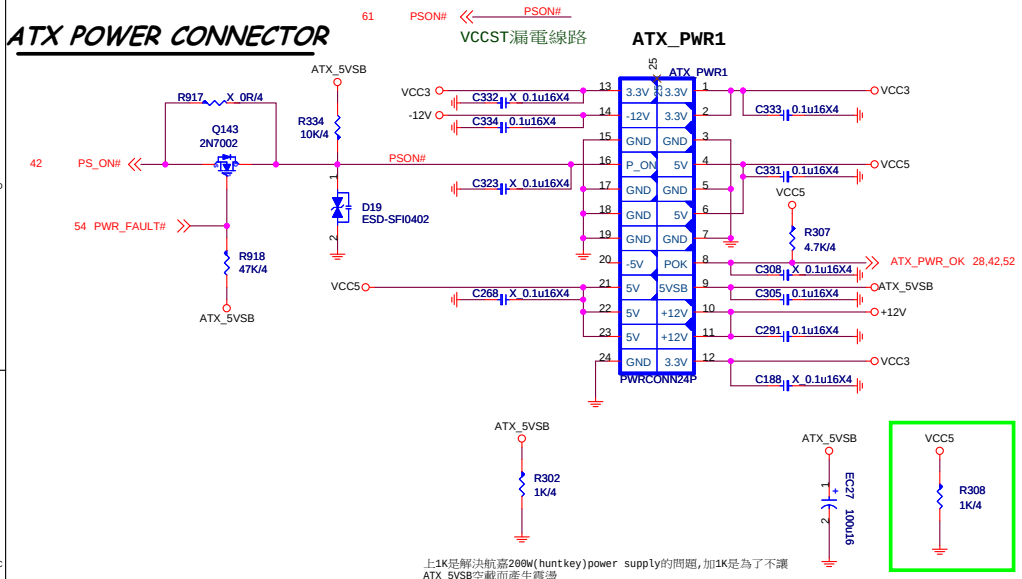
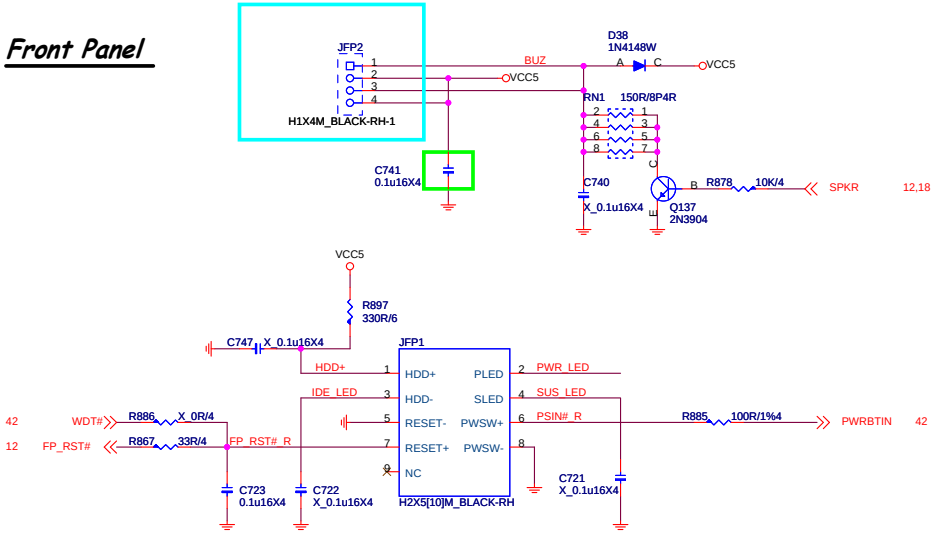
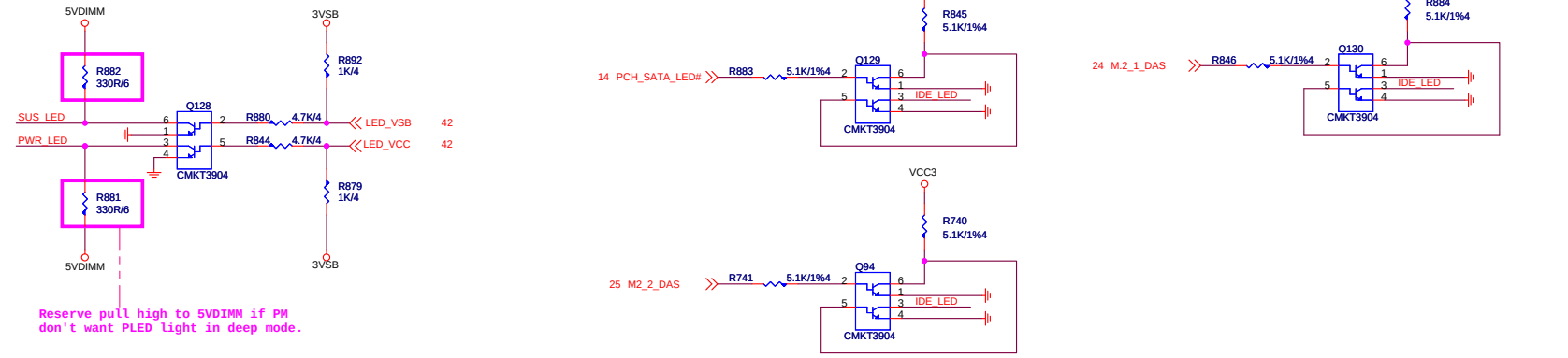
ATX POWER CONNECTOR



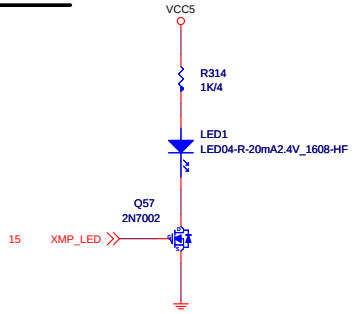
Front Panel



LED

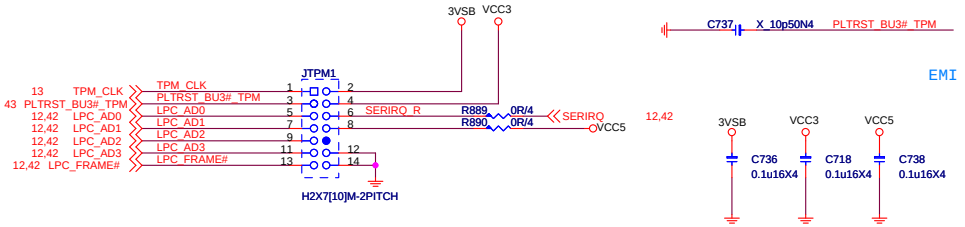


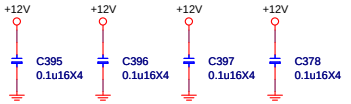
XMP LED



TPM

Confirm ESPI TPM card and TPM card pin difine
(Not ready)





MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	ATX Power/F_Panel	10

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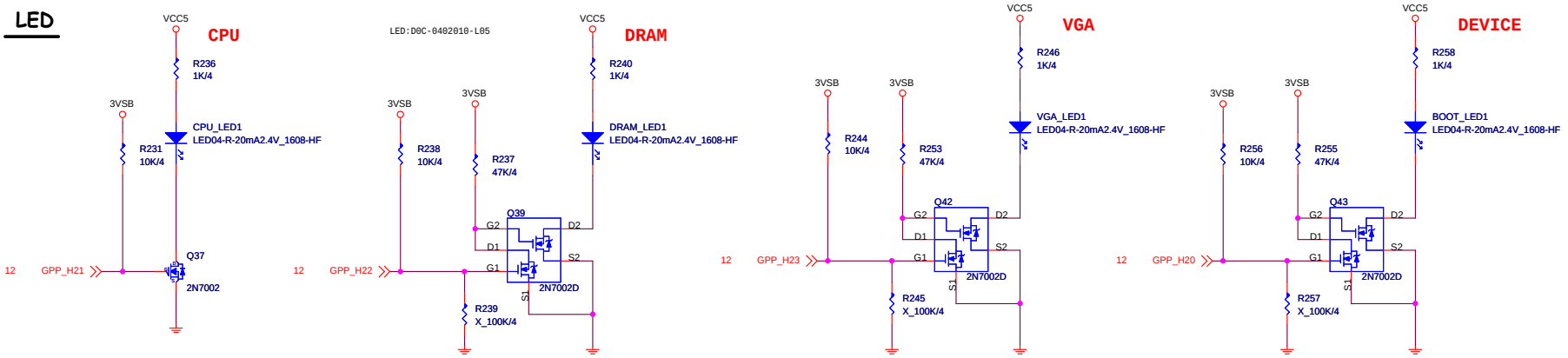

關機斷電狀態下，4個LED先維持default全暗，開機通電後：

1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED減掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED減掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED減掉。
4. 因此最後正常順利開機後，三個LED燈都是滅掉的。
   （系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

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MS-7A63

Size: Custom | Document Description: EZ DEBUG LED | Rev: 10

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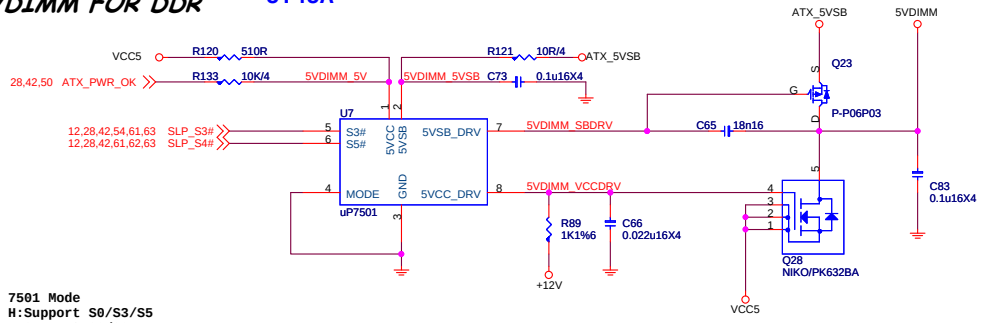
5VDIMM FOR DDR

5.45A

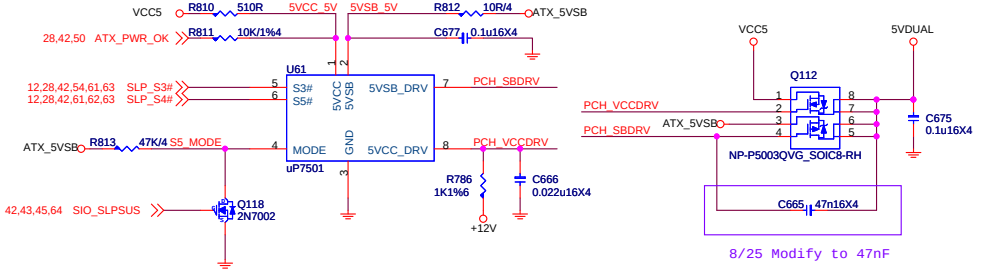


7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

5VDUAL

5VDUAL is power source of 1P0SB

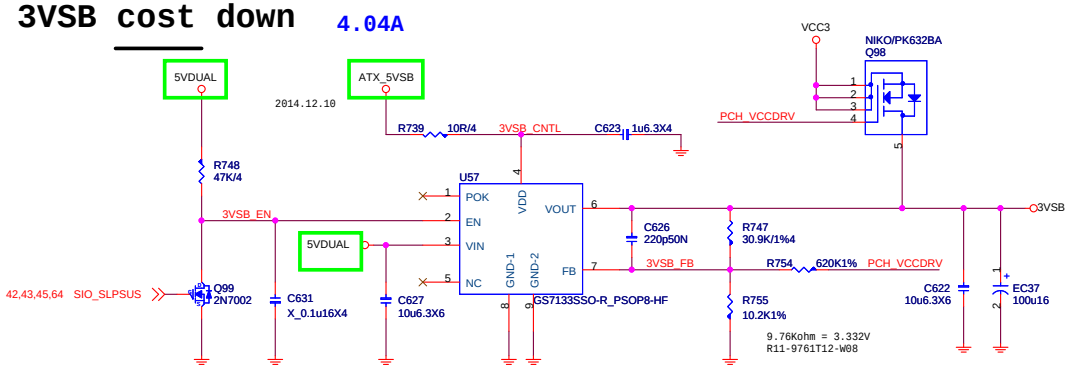
PCH:2.95A
3VSB:4.04A
MAX:6.99A



8/25 Modify to 47nF

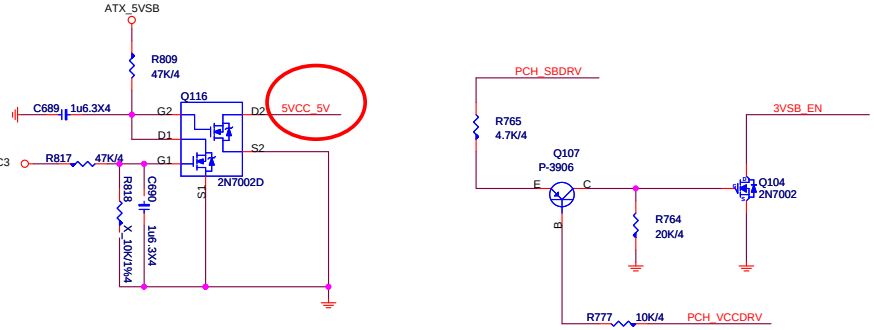
3VSB cost down

4.04A



AVL:I31-3730S02-N62 2014.10.15 update

VFB=3.224V for S0->S3 3VSB voltage raise & ATX_5VSB drop.

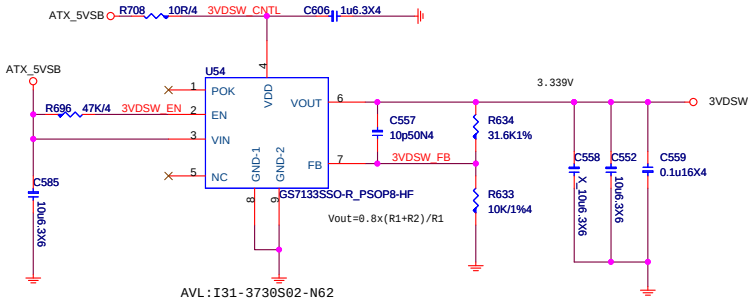


3VSB_EN >> 3VSB_EN 44

防G3-->S5底下5VSBDRV2瞬間有電變沒電,使得下一級電壓爬升有drop

3VDSW

0.422A



AVL:I31-3730S02-N62

3VDSW_EN >> 3VDSW_EN 44

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Size	Document Description	Rev
Custom	ACPI UPI	10

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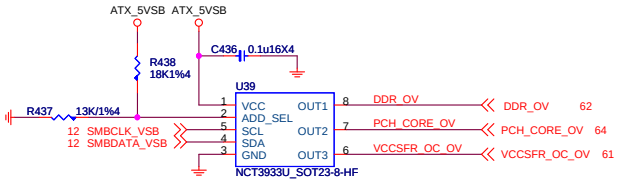
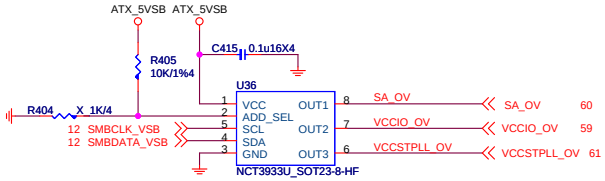
UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



0x20:RH=10K,RL=OPEN



ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

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Size: Custom | Document Description: OV-NCT3933/GPIO-NCT5605 | Rev: 10

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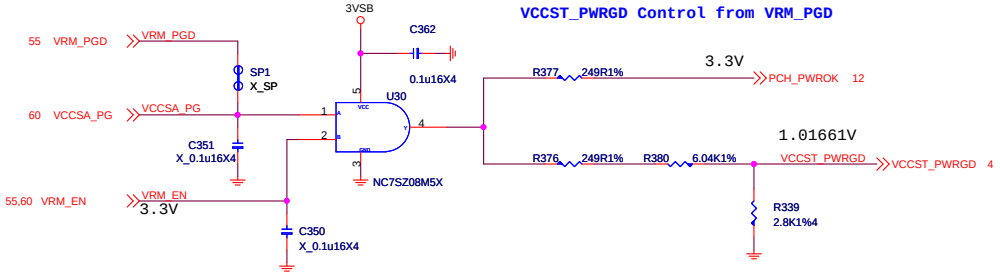
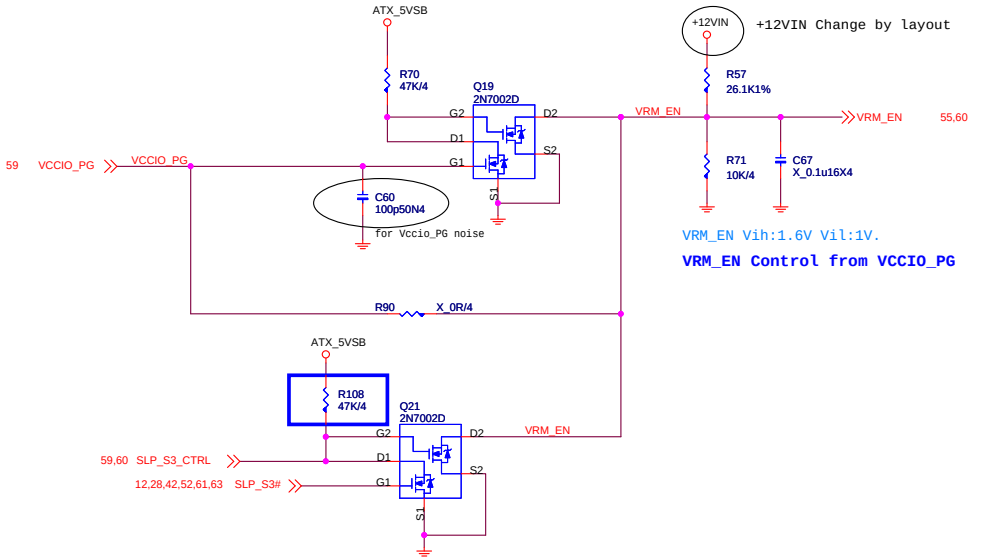
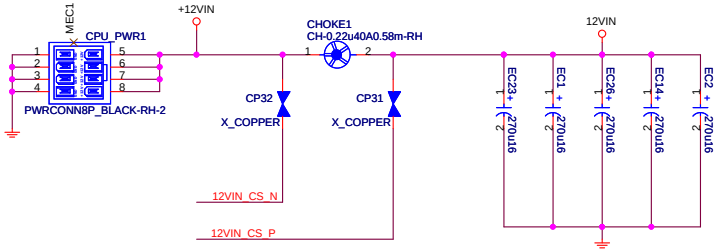
VCCSA&Vcore use same PWM IC, pull up VCC3
VCCSA&Vcore use different PWM IC,pull up VCCSA
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.

PCH_PWROK Control from VCCIO_PG&VCCSA
VCCST_PWRGD Control from VRM_PGD

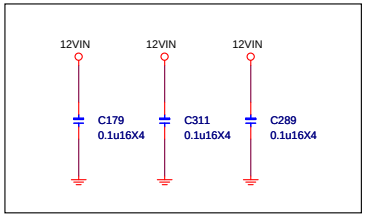


VRM_EN Control from VCCIO_PG

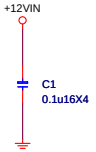


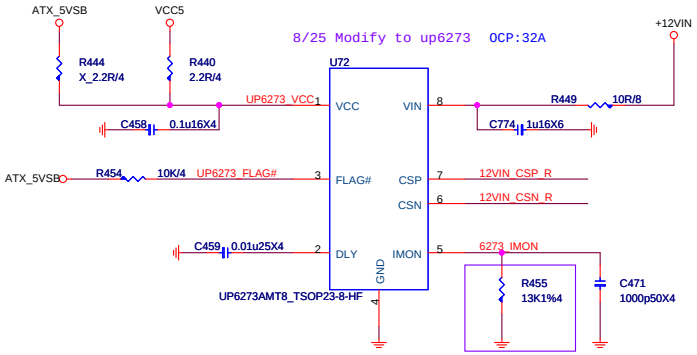


Iripple=30.95A
VCORE 18.101A
VGT 8.457A
VCCSA 4.392A

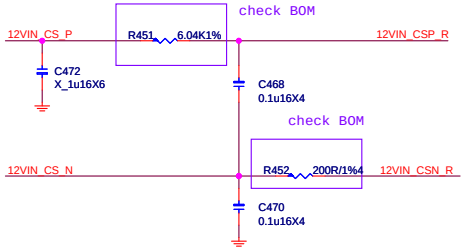


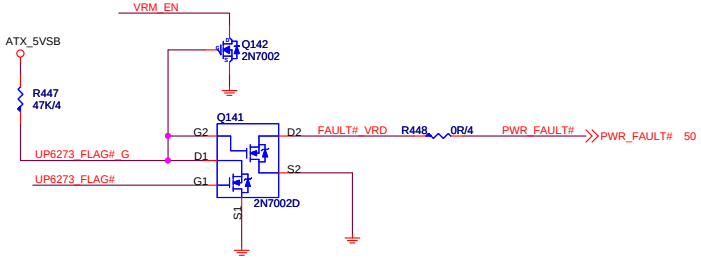
CLose to JPWR2





Iin=(Vmon*Rcsn)/(Rmon*Rdc) check BOM
Vmon=1.2
can change OCP trigger level by Rcsn and Rmon





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Vcore: ICC Max 100A
LL: 2.1 mohm
OCP: 200A

VGT: ICC Max 48A
LL: 3.1 mohm
OCP: 75A

U8

teknisi indonesia

close to VRM < 0.1"

close to VRM <0.1"

MICRO-STAR INT'L CO.,LTD	
MS-7A63	
Size: Custom	Document Description: PWM-UP9508 VCORE+VGT
Rev: 10	
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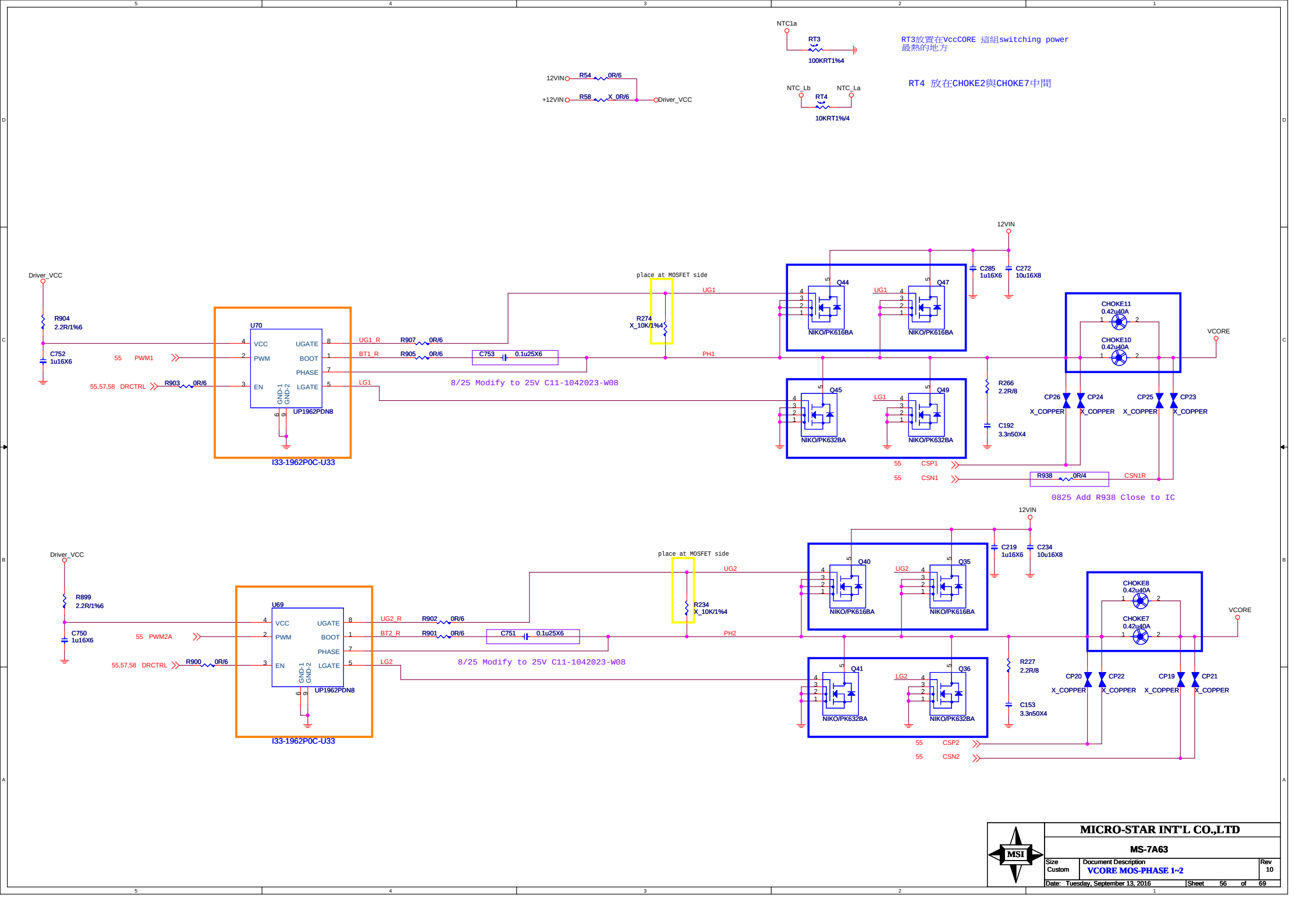

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A63	
Size: Custom	Document Description: VCORE MOS-PHASE 1~2	Rev: 10
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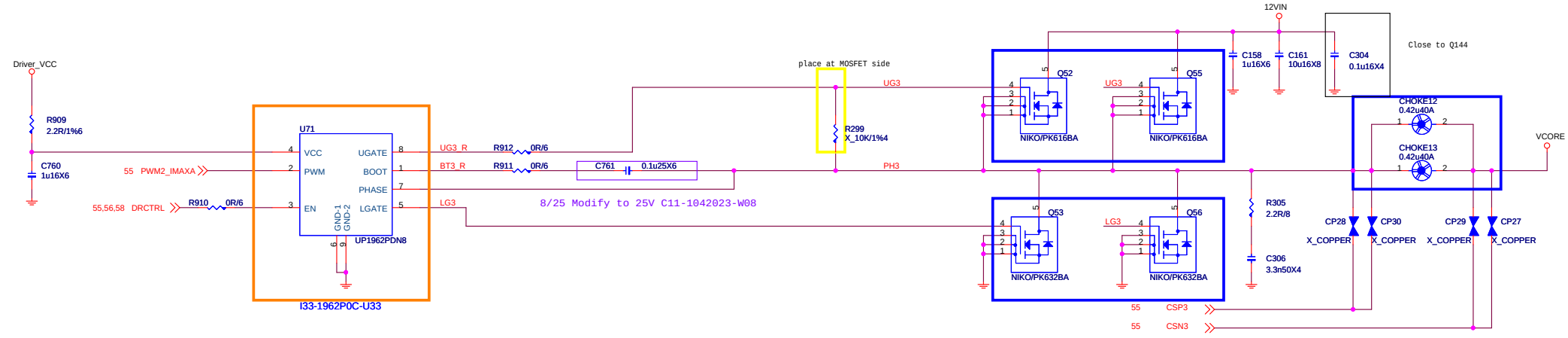
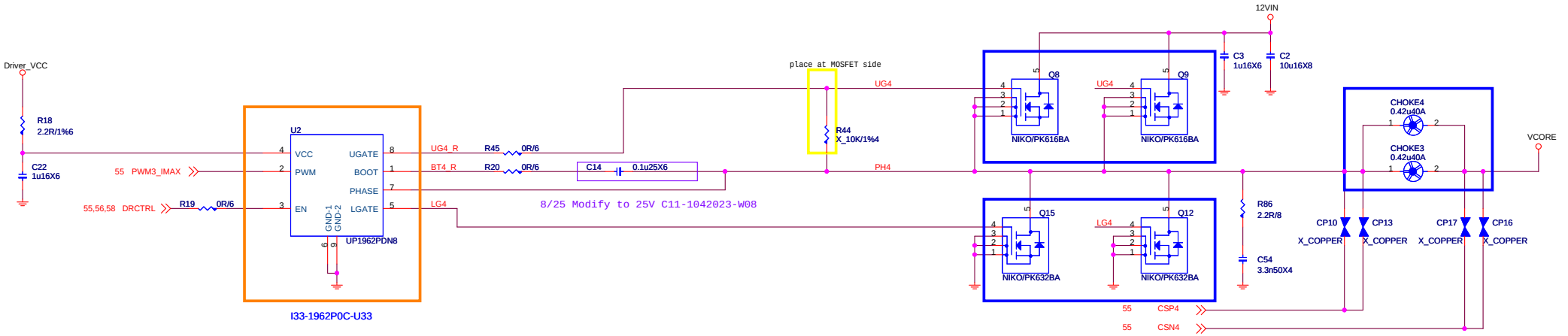
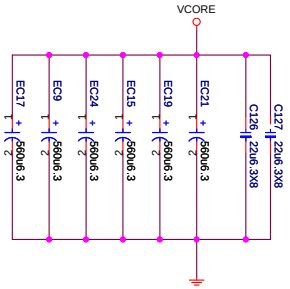


Vinafix.com





MICRO-STAR INT'L CO.,LTD	
MS-7A63	
Size: Custom	Document Description: VCORE MOS-PHASE 3~4
Rev: 10	
Date: Tuesday, September 13, 2016	Sheet 57 of 69

RT2 放在L50與L52中間

RT1放置在VccGT 這組switching power 最熱的地方

NTCA_Lb NTCA_La RT2 10KRT1%/4

NTCA1a RT1 100KRT1%/4

12VIN

C5 1u16X6 C4 1u16X6

place at MOSFET side

UG1A_R R106 0R/6 UG1A

R46 X_10K/1%4

Q10 NIKO/PK616BA

BT1A_R R107 0R/6 C71 0.1u25X6 PH1A

8/25 Modify to 25V C11-1042023-W08

LG1A

Q13 NIKO/PK632BA

Q16 NIKO/PK632BA

R87 2.2R/8

C55 3.3n50X4

CHOKE5 0.22u60A

VGT

CP12 X_COPPER

CP15 X_COPPER

ISP1 R104 X_0R/4

ISP2 R118 0R/4 ISEN1A-1

55 CSP1A-1 R103 5.6K/1%4 CSP1A-1

C70 1000p50X4 CSN1A-1

55 CSN1A-1

12VIN

C7 10u16X8 C6 10u16X8

place at MOSFET side

UG2A_R R153 0R/6 UG2A

R47 X_10K/1%4

Q11 NIKO/PK616BA

BT2A_R R152 0R/6 C89 0.1u25X6 PH2A

8/25 Modify to 25V C11-1042023-W08

LG2A

Q14 NIKO/PK632BA

Q17 NIKO/PK632BA

R88 2.2R/8

C56 3.3n50X4

CHOKE6 0.22u60A

VGT

CP11 X_COPPER

CP14 X_COPPER

ISP1 R119 0R/4

ISP2 R132 X_0R/4 ISEN1A-2 ISEN1A-2

55 CSP1A-2 R117 5.6K/1%4 CSP1A-2

C81 1000p50X4 CSN1A-2

55 CSN1A-2

D9 S-BAT54A_SOT23 BT1A_R BT2A_R

Driver_VCC

R151 2.2R/1%6

C88 1u16X6

U6

VCC BOOT1 ISP1 UG1 ISP2 PH1 PWM0 LG1 EN BOOT2 ISP0 UG2 NC PH2 GND LG2 GND

55 PWM1A 55,56,57 DRCTRL R105 0R/6 55 CSP1A CSP1A

BT1A_R UG1A_R PH1A LG1A BT2A_R UG2A_R PH2A LG2A

uP1961SQDD_WQFN16-HF

I33-1961S0C-U33

EC5 EC7 EC10 EC11 EC6 560u6.3

VGT

VCCIO

0.95V; 5.5A

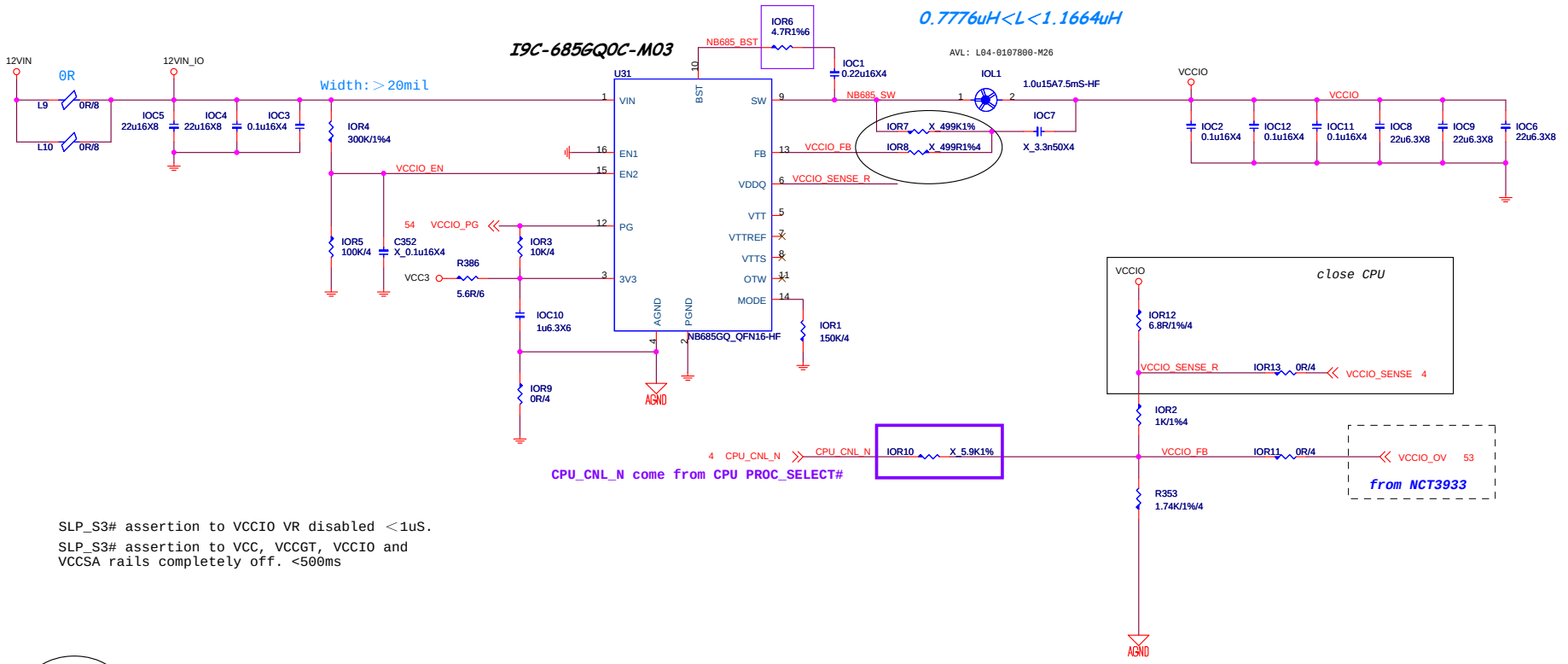
IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

support OV=>NB685

0902 Modify IOR6 to 0603 Size

0.7776uH<L<1.1664uH

I9C-685GQ0C-M03

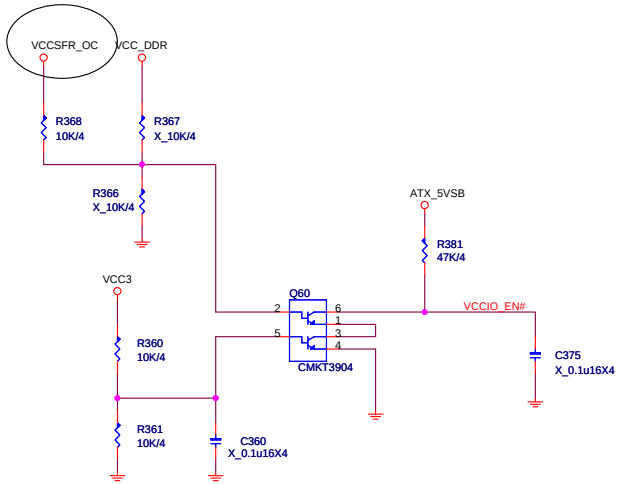


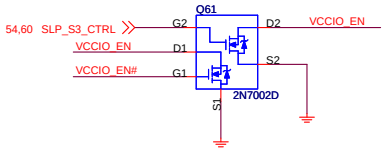
4 CPU_CNL_N CPU_CNL_N IOR10 X_5.9K1%

CPU_CNL_N come from CPU PROC_SELECT#

SLP_S3# assertion to VCCIO VR disabled <1uS.

SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off. <500ms





SLP_S3# assertion to VR disabled
max:1us

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Size: Custom	Document Description: CPU PWR_VCCIO	Rev: 10
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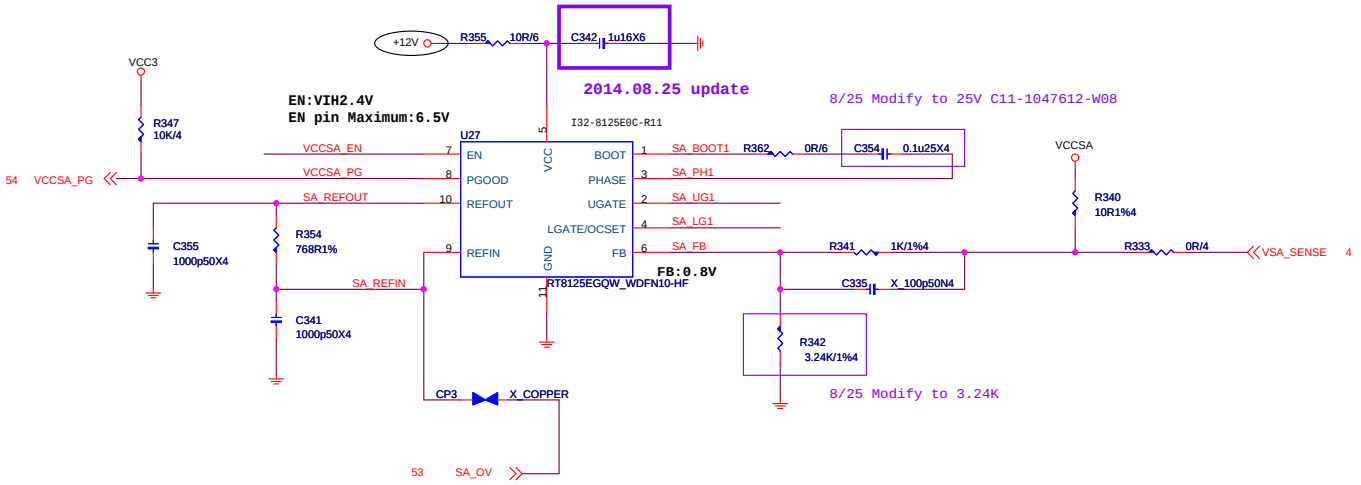
SA Power:1.05V,11.1A

*OCP =11.1A*1.4=15.54A*
*Rocs(R417)=OCP*Rdson(Low side)3.4mohm]/10uA*
=15.54(3.4)mohm/10uA*
=5.2836Kohm

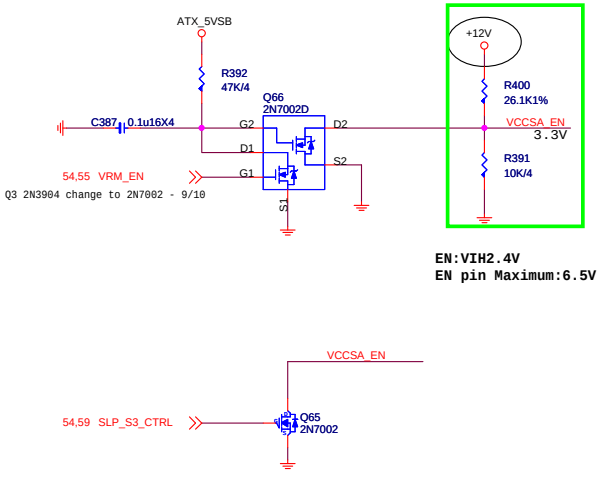
Rocs:5.2836K,OCP:
D03-4C05N03-O05 : 15.76A
D03-632BA0C-N03 : 16.24A
use UBIQ MOS need Check

Rdson(low)10V
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm



VRM_EN線路update

Pull up by layout&Check level



SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.

SLP_S3# assertion to VR disabled
max:1us

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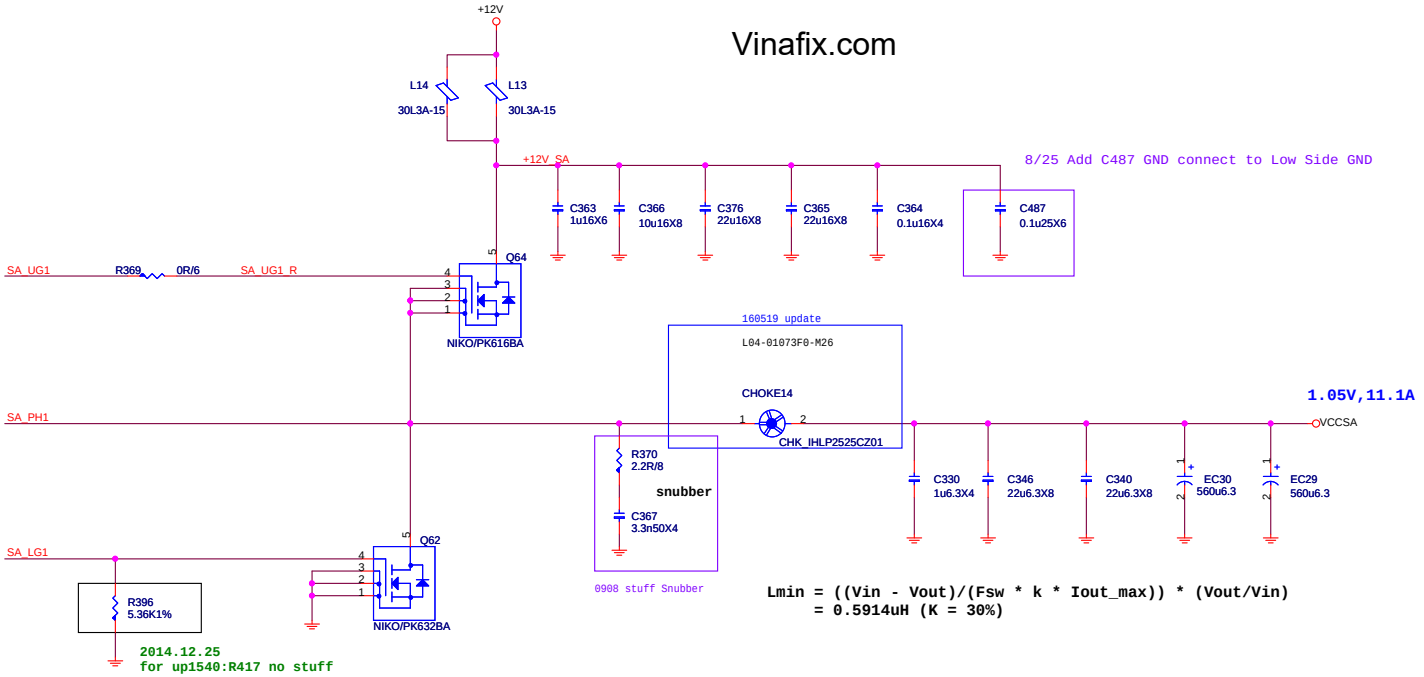

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MS-7A63

Size	Document Description	Rev
Custom	CPU PWR_SA-RT8125C	10

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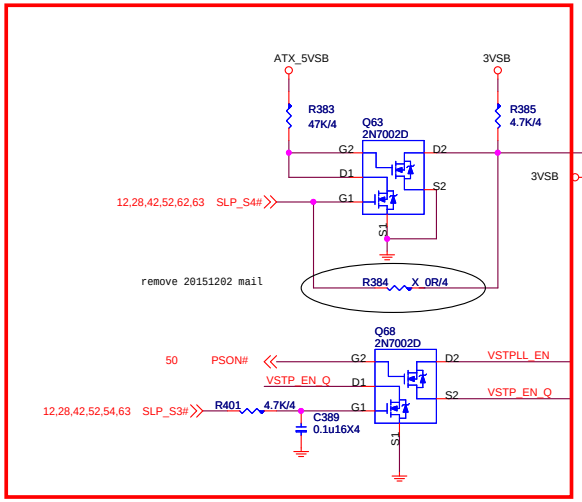
VCCST

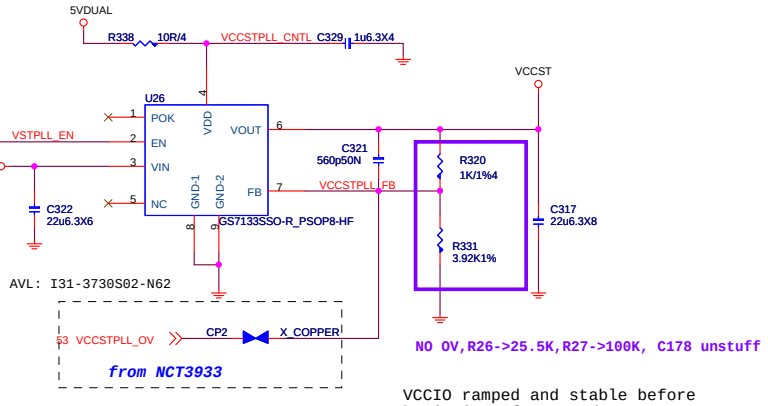
for Gaming3/5, Classic, ECO and H110

VCCST:60mA
VCCPLL:150mA

1.0V; 210mA

For Cost down VCCST&VCCPLL merge





NO OV,R26->25.5K,R27->100K, C178 unstuff

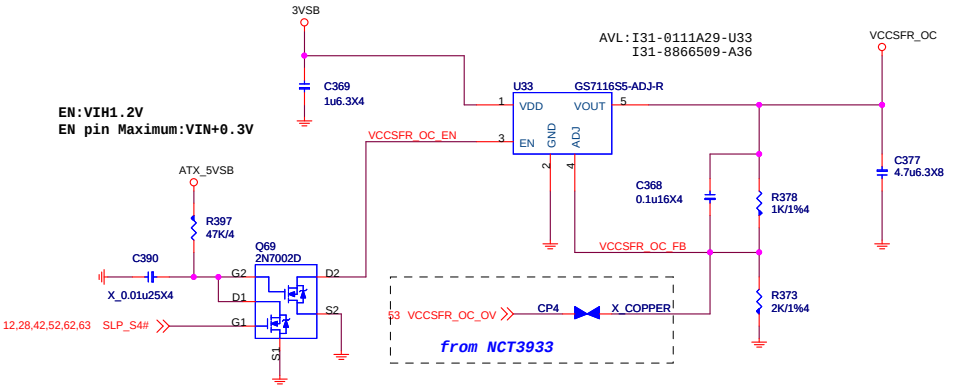
VCCIO ramped and stable before beginning of VCCOPC/VCCEOPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD

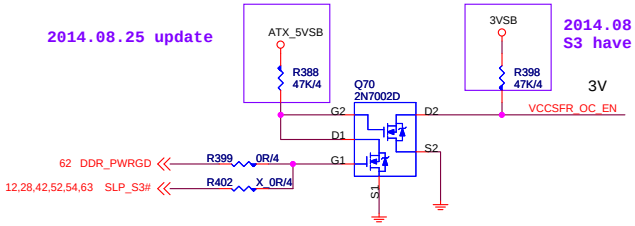
VCCPLL_OC

1.2V; 130mA

2014.08.21 update



2014.08.25 update



2014.08.25 update
S3 have power

MICRO-STAR INT'L CO.,LTD

MS-7A63

Size	Document Description	Rev
Custom	CPU PWR_ST/PLL	10

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DDR4_1.2V 2.5A+9.5A+1.2A=13.5A

2.8A FOR CPU

9.5A FOR 4DIMM

1.2A FOR DDR VTT

OCP =13.2A*1.5=20.25A

Rocs(R95)=OCP*Rdson[(Low side)]/10uA

=20.25A*(4.6)mohm/10uA

=9.315Kohm

Rocpset:5.1K

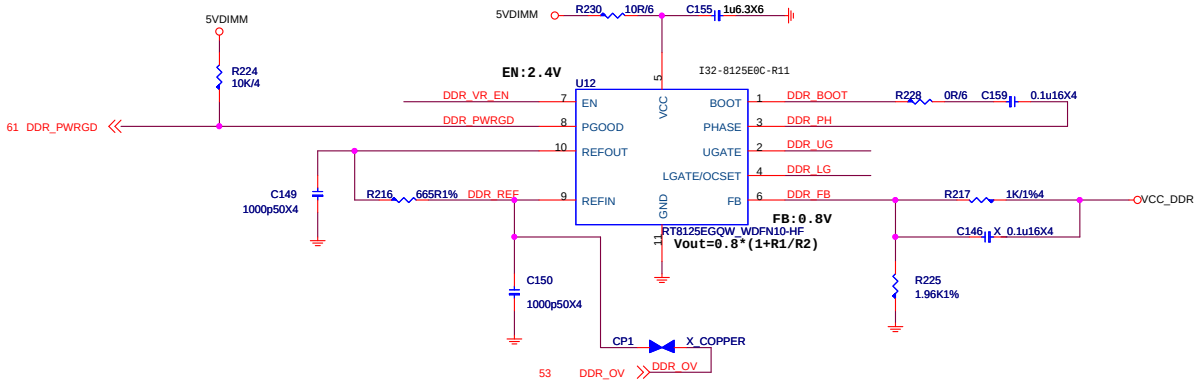
OCP=Rocset*Rdson[(Low side)]/10uA

=9.31K*(4.6)mohm/10uA

=20.23A

use UBIQ MOS need Check

Rdson(low)4.5V
D03-4C05N03-O05 : 5 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm



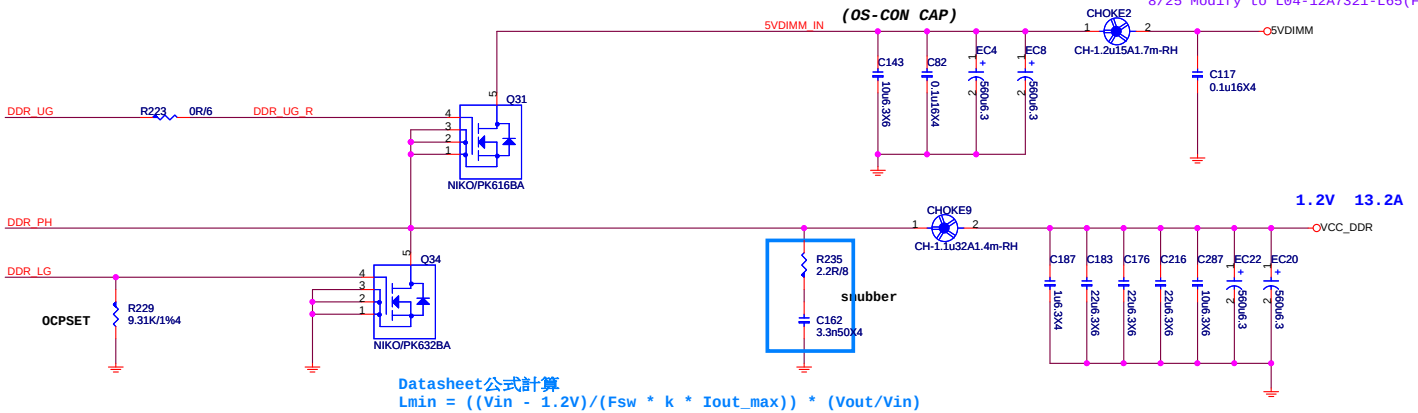
Irms = Iout * SQRT{(Vout/Vin) * [1 - (Vout/Vin)]}

= 13.2* 0.427

= 5.636A

(OS-CON CAP)

8/25 Modify to L04-12A7321-L65(F)



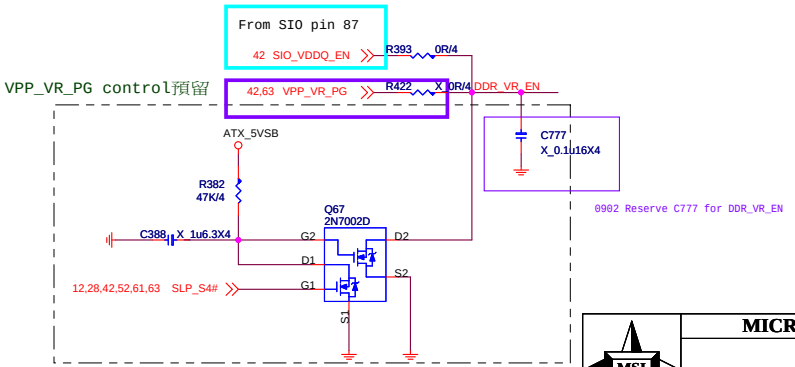
Datasheet公式計算

Lmin = ((Vin - 1.2V)/(Fsw * k * Iout_max)) * (Vout/Vin)

= 0.7677uH (K = 30%)

若帶入CAP ESR計算,0.2432uH＜L＜1.2897uH

2014.12.17 update



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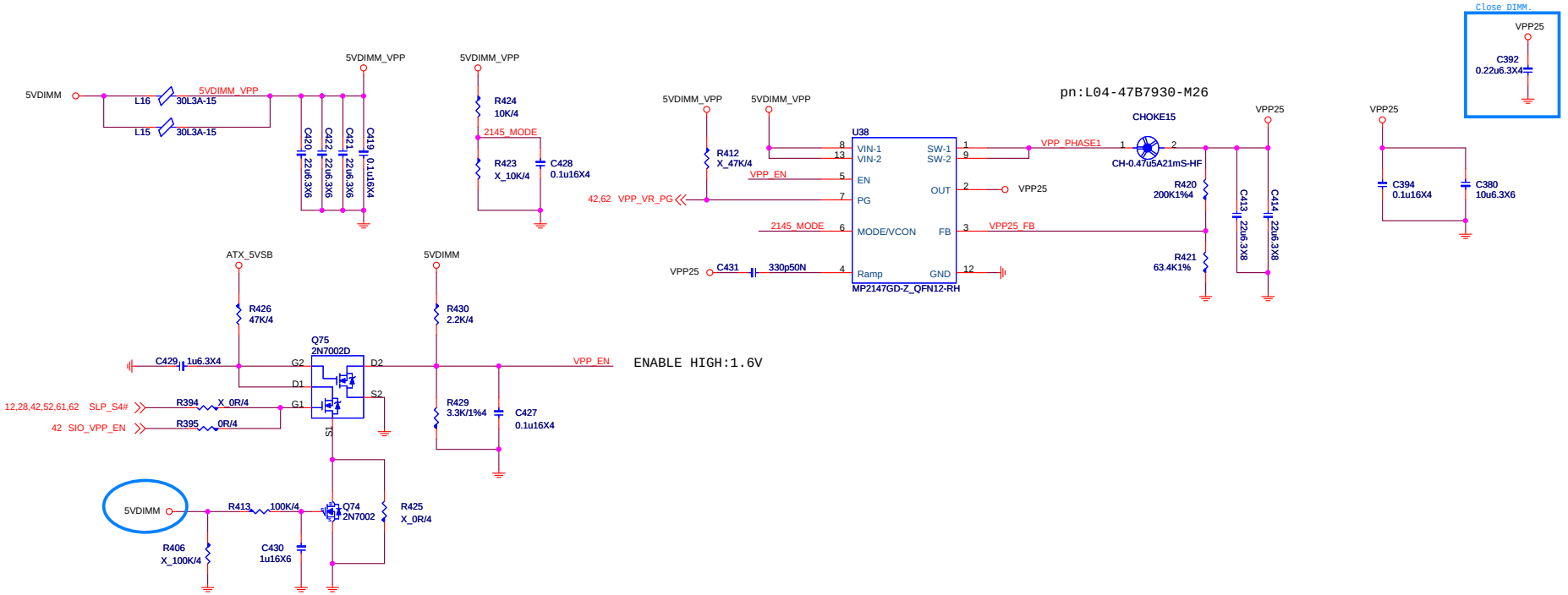
MS-7A63		
Size: Custom	Document Description: DDR4 Power-RT8125C	Rev: 10
Date: Tuesday, September 13, 2016	Sheet 62 of 69	

4DIMM :2.24A FOR DDR VPP2.5V

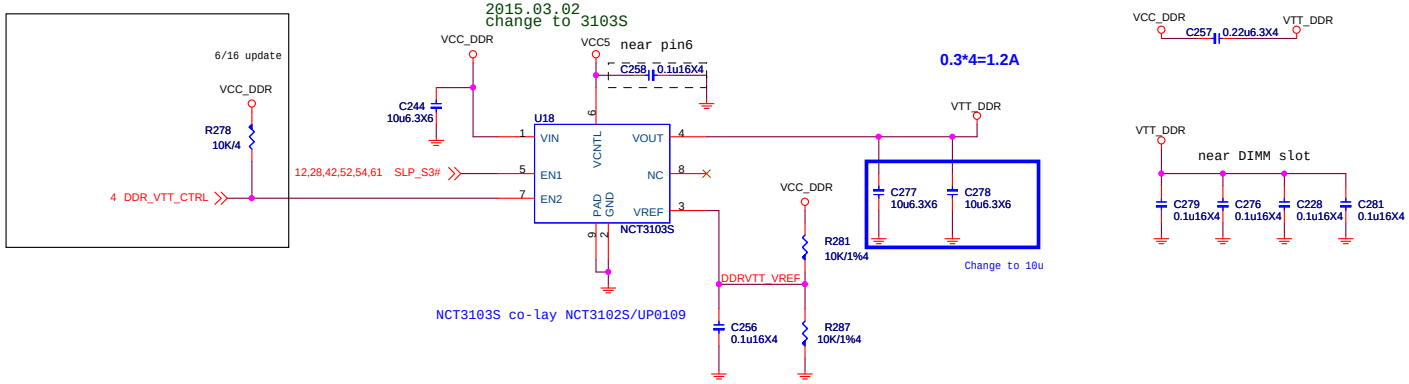
VPP25 Power

2.5V; 2.24A



To make sure VPP EN after 5VDIMM stable

DDR VTT Power



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PCH_1VSB

1.0V; 11.83A

OCP = 17.745A

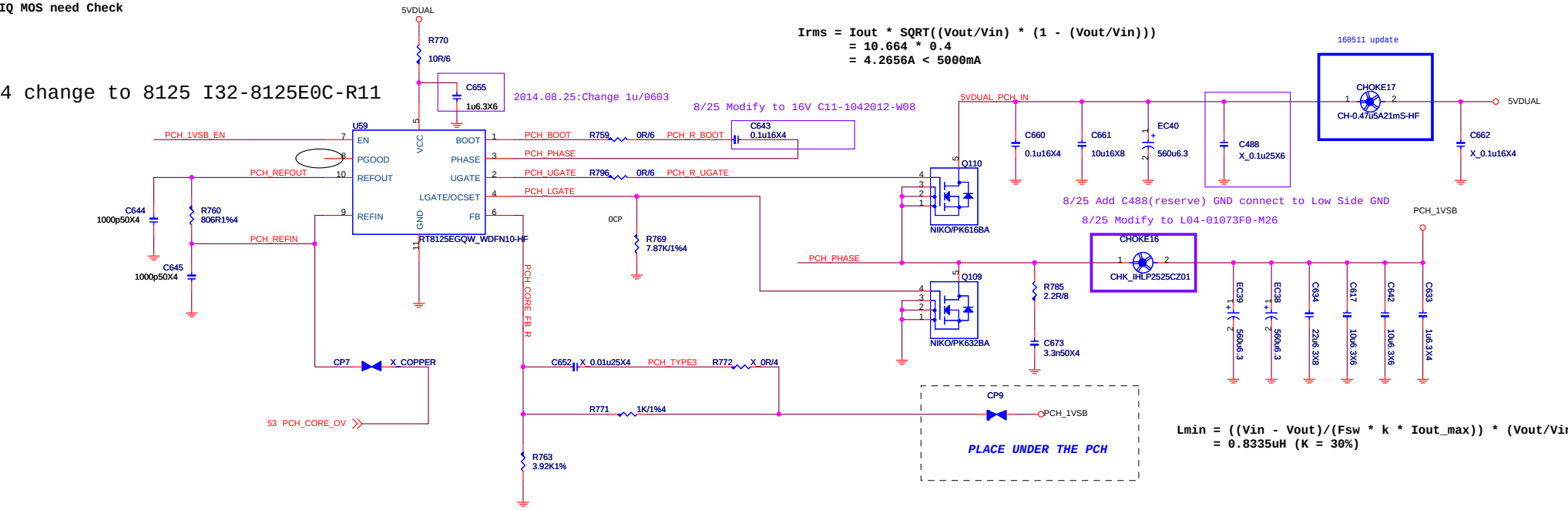
Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 1.5 * 11.83 * 4.6mohm / 10uA
= 8.16K

Rocs:7.87K,OCP:
D03-4C05N03-005 : 15.74A
D03-632BA0C-N03 : 17.1A
use UBIQ MOS need Check

Rdson(low)4.5V
D03-3116M00-U47 : 3.6 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm

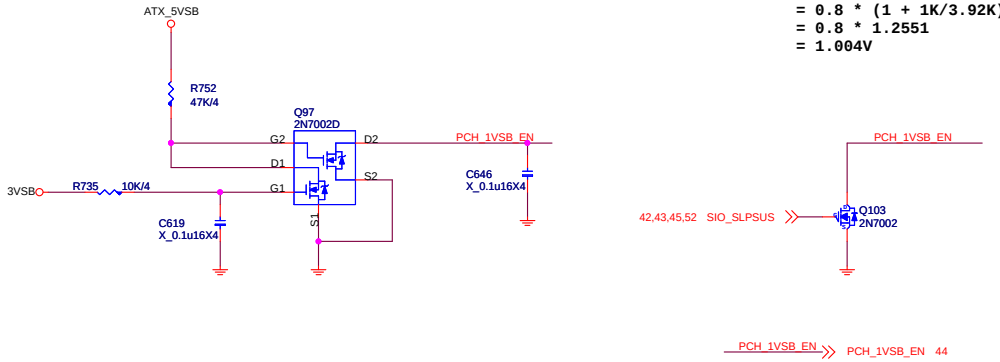
1504 change to 8125 I32-8125E0C-R11

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 10.664 * 0.4
= 4.2656A < 5000mA



Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)

Vout = Vref * (1 + R821/R822)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V



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PCB

PCB1

7A63_10

PD0-07A6310-G37

PD0-07A6310-E48

MK_LABLE1 — MARKET LABLE — MK_LABLE1

AMI_LABLE — AMI_BIOS LABLE — BIOS_LABLE

HDMI_LABLE — HDMI LABLE — HDMI LABEL

CFOS_LABLE — CFOS LABLE — CFOS_LABLE

NAHIMIC_LABLE — NAHIMIC LABLE — NAHIMIC_LABLE

SSE_LABLE — SSE LABLE — SSE_LABLE

USB31 — USB3.1 LABLE — X_USB31_LABLE

Audio Small Cover

COVER1 — Audio Cover — E21-7978010-RH

CPU_H1 — CPU 鐵座 — CPU_H1

BAT1_X1 — BAT-BCR2032P-RH

Mounting Holes

MH1, MH2, MH3, MH4, MH5, MH6, MH7, MH8, MH9 — X_MH001

C691 0.1u16X4

C714 0.1u16X4

HS_MOS1 — MEC1, MEC2, MEC3, MEC4, MEC5, MEC6, MEC7 — X_mosheatsink

PCH_HS1 — MEC1, MEC2 — HS-0408530-RH

DDR_COVER1 — DDR COVER — X1, X2, X3, X4, X5 — E21-7A63010-RH

VR_COVER1 — VR Cover — X1, X2 — E21-7A63020-RH

E21-7A63020-A91

Change footprint

0901 Modify DDR_COVER1 PIN X1.X2.X3.X4.X5 Connect to GND

Simulation

VCC5 — SIM1 — X_PIN1*2

SIM2 — X_PIN1*2

Test point

VCORE, VGT, VCC_DDR, VCCSA, VCCIO, PCH_1VSB, VCCST, VCCSFR_OC, VTT_DDR, VPP25

VCORE1, VGT1, VCC_DDR1, VCCSA1, VCCIO1, PCH_1VSB1, VCCST1, VCCSFR1, VTT_DDR1, VPP1

Optical Fiducial Marks-120

FM1, FM2, FM3, FM4, FM5, FM6, FM7, FM8 — X_FM

HS_MOS2 — MEC1, MEC2 — HS-0503710-RH

HS_MOS3 — MEC1, MEC2 — HS-0503720-RH

PCH_HS — MEC1, MEC2 — X_PCH_HS

EMI CAP

VCC5 — C772 X_0.1u16X4

VCC5 — C773 X_0.1u16X4

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